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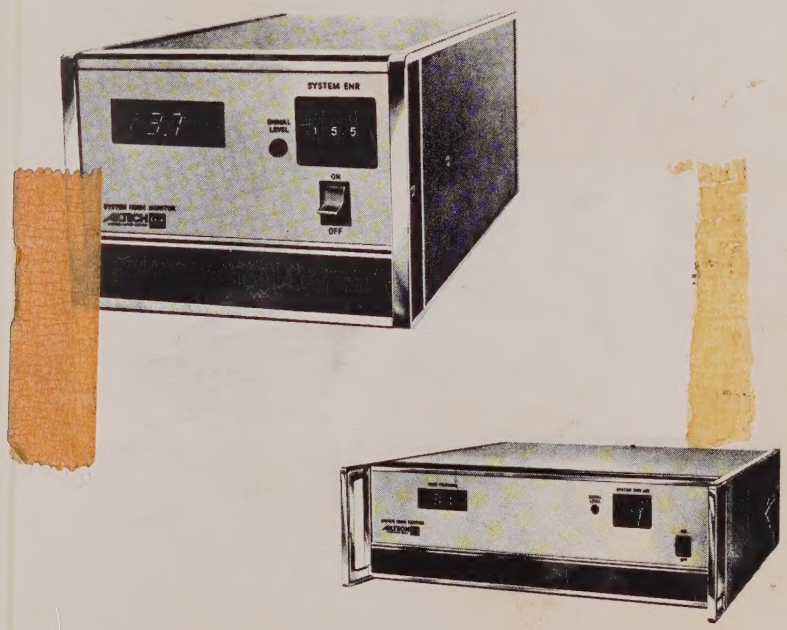
OPERATION AND SERVICE MANUAL

7360
7370

SYSTEM NOISE MONITORS



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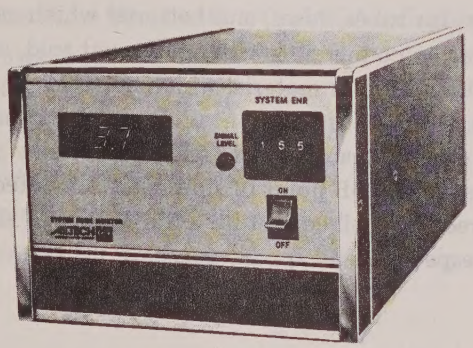

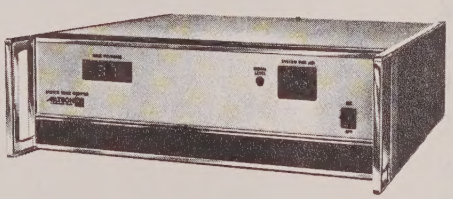

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WARRANTY

Except for tubes, fuses, and batteries which carry no warranty, Cutler-Hammer, in connection with equipment sold, agrees to correct any defect in workmanship or material which may develop during the period of one year from the date of shipment under proper or normal use and not in excess of the original manufacturer's life expectancy ratings, by its option to repair or replace, FOB point of shipment, the defective part or parts, and such correction shall constitute a fulfillment of all Cutler-Hammer liabilities in respect to said apparatus.

TABLE OF CONTENTS

		Page
Chapter I--General Information		
1-1.	Introduction	1-1
1-3.	General Description	1-1
1-7.	Safety Precautions	1-1
1-10.	Technical Specifications	1-1
1-12.	Functional Description	1-5
1-13.	General	1-5
1-15.	The Noise Monitor in a Typical Application	1-5
1-17.	Auxiliary Outputs	1-6
1-19.	Options	1-7
1-21.	Accessories	1-7
1-22.	Noise Generators	1-7
1-23.	Precision Attenuation	1-9
1-24.	Test Equipment	1-10
Chapter II--Installation		
2-1.	Introduction	2-1
2-3.	Unpacking, Inspection and Damage Claims	2-1
2-5.	Ancillary Items	2-1
2-7.	Rack Mounting	2-1
2-9.	Preparation for Use	2-1
2-11.	Initial Checkout	2-2
2-14.	General	2-2
2-16.	Checkout Procedures	2-2
Chapter III--Operating Instructions		
3-1.	General	3-1
3-3.	Description of Operating Controls, Indicators and Connectors	3-1
3-5.	Set-up Procedures	3-1
3-8.	Interconnections	3-1
3-17.	Excess Noise Ratio Setting	3-5
3-21.	Establishing the Correct Signal Levels	3-5
3-27.	Operation	3-7

		Page
3-29.	Use of Auxiliary Outputs	3-9
3-31.	Signal Monitor, J1, Pin 4	3-9
3-33.	External Meter, J1, Pins 6 and 7	3-9
3-35.	Recorder Output, J1, Pin 8	3-10
3-37.	Digital Outputs, J1, Pins 12 and 16 thru 24	3-10
3-40.	Manual Noise Figure (Temperature) Measurements	3-11

Chapter IV--Theory of Operation

4-1.	Introduction	4-1
4-3.	General Theory	4-1
4-4.	Noise Figure Theory	4-1
4-6.	Noise Figure Measurement	4-2
4-8.	Operating Noise Figure and Temperature Measurement	4-4
4-11.	Functional Description (Automatic Noise Measurement)	4-5
4-15.	Circuit Descriptions	4-9
4-17.	IF Amplifier	4-9
4-22.	Square Law Detector	4-9
4-24.	Variable Gain Amplifier	4-9
4-25.	Synchronous Integrator and Meter Amplifier	4-9
4-27.	AGC Amplifier	4-10
4-31.	Timing Signal Generator	4-10
4-39.	Power Supply Board	4-12
4-41.	+12 Volt Regulator	4-12
4-42.	-12 Volt Regulator	4-12
4-43.	+28 Volt Noise Source Supply	4-12
4-44.	+5 Volt Regulator	4-12
4-45.	Digital Noise Figure Circuits	4-12
4-46.	Operational Description	4-12
4-59.	Detailed Digital Circuit Descriptions	4-16
4-61.	Variable Gain Operational Amplifier	4-16
4-64.	Ramp Generator	4-19
4-65.	Comparator	4-19
4-66.	High Frequency Clock	4-19
4-68.	HF Clock Control	4-19
4-69.	Ramp Control	4-19
4-71.	Master Clock	4-20
4-72.	Control Logic	4-20

			Page
	4-74.	Gain Control Logic	4-20
	4-76.	Data Output Circuit	4-20
Chapter V–Maintenance and Adjustments			
5-1.	General		5-1
5-3.	Performance Verification		5-1
	5-6.	Minimum Operating Level	5-1
	5-7.	Noise Generator Power	5-2
	5-8.	Accuracy	5-2
5-10.	Checks and Adjustments		5-3
5-13.	Power Supply Adjustments		5-5
5-14.	IF Adjustments		5-6
	5-16.	Preliminary	5-6
	5-17.	Procedure	5-7
5-18.	Calibration Adjustments		5-7
5-20.	Digital Adjustments		5-7
	5-24.	Initial Settings	5-8
	5-27.	Calibration Settings	5-8
	5-28.	Ramp Slope	5-8
	5-29.	H.F. Clock Frequency	5-8
	5-30.	High Noise Breakpoint	5-8
5-31.	Auxiliary Output Adjustments		5-8
	5-33.	Signal Monitor	5-9
	5-34.	Recorder Output	5-9
5-35.	Troubleshooting		5-9
5-37.	General Information		5-9
	5-38.	Tools	5-9
	5-39.	Transistors	5-9
	5-40.	Integrated Circuits	5-9
	5-41.	Logic Family	5-9
	5-44.	Logic Gates	5-10
	5-45.	Analog Switches	5-10
	5-47.	Flip-Flops	5-10
	5-48.	Operational Amplifiers	5-10
	5-49.	Printed Circuit Boards	5-10
	5-51.	Printed Circuit Board Connectors	5-18
	5-52.	Front Panel Lamps	5-19
	5-53.	ENR Thumbwheel Switch	5-19

		Page
5-54.	Troubleshooting Procedures	5-19
5-57.	Factory Service	5-19

Chapter VI--Spare Parts

6-1.	General	6-1
6-2.	Recommended Spare Parts	6-1
6-3.	Replaceable Spare Parts	6-1

LIST OF ILLUSTRATIONS

Figure		Page
Frontis-piece		
1-1	Digital System Noise Monitors	1-2
1-2	SNM, Model 7360 Outline Dimensions	1-3
1-3	SNM, Model 7370 Outline Dimensions	1-3
1-4	Typical Noise Figure Measurement Set-up Using the AILTECH 7300 System Noise Monitors	1-5
1-5	Layout of J1	1-6
1-6	Typical Noise Sources Used with the 7300 SNM's	1-8
1-7	7650/7660 Maximum ENR vs Frequency	1-9
1-8	AILTECH 32 Precision Attenuator (Cased Version)	1-10
3-1	7360/7370 SNM Control, Indicator, Connector Locations	3-3
3-2	Bench Measurement Set-ups	3-4
3-3	Typical "Operating" Measurement Set-up	3-4
3-4	Illustration of Sensitivity and Signal Level Range	3-6
3-5	Location of the Manual-Auto Controls	3-8
3-6	AILTECH Noise Figure Slide Rule	3-10
3-7	Nomograph for Determining Noise Figure or Temperature	3-12
3-8	BCD Data Output Strobe	3-13
4-1	Equivalent Noise Representation of a Noisy Network	4-3
4-2	Equivalent Representation of Noise Figure Measurement Set-up	4-3
4-3	Equivalent Representation of an Operating Noise Measurement	4-4
4-4	Functional Block Diagram	4-7
4-5	Digital Circuitry, Simplified Block Diagram	4-13
4-6	Digital Circuit, Simplified Timing Diagram	4-17
4-7	Control Logic, Detailed Timing Diagram	4-21
5-1	Set-up for Checking SNM Accuracy	5-3
5-2	Adjustment Locations	5-4
5-3	Plastic-Case Transistors	5-7
5-4	Integrated Circuit Case Styles	5-11
5-5	Integrated Circuits Functional Illustrations	5-15
5-6	3-Input Logic Gate Operation	5-17
5-7	Operation of the COS/MOS Bilateral Switch	5-17
5-8	Typical Applications of Operational Amplifiers	5-18
5-9	Pin Numbering Layout of a Typical AMP 87133 Connector	5-18
5-10	General Troubleshooting Chart	5-21
5-11	IF Troubleshooting Chart	5-23

Figure		Page
5-12	AGC Troubleshooting Chart	5-25
5-13	Video-DC Troubleshooting Chart	5-27
5-14	Timing Generator Troubleshooting Chart	5-29
5-15	Power Supply Troubleshooting Chart	5-31
5-16	Digital/Display Troubleshooting Chart	5-33
5-17	Power Supply, Parts Location and Schematic Diagrams	5-38
5-18	IF-Video Parts Location and Schematic Diagrams	5-41
5-19	Digital Parts Location and Schematic Diagrams	5-45
5-20	Display Parts Location and Schematic Diagrams	5-49
5-21	Wiring Diagram	5-51

LIST OF TABLES

Table		Page
1-1	Technical Specifications	1-4
1-2	Applicable Noise Sources	1-7
1-3	Recommended Test Equipment	1-10
3-1	AILTECH 7360/7370 System Noise Monitors Controls, Indicators and Connectors	3-2
3-2	BCD Outputs	3-11
4-1	Functional Illustration — Timing and Gating	4-8
4-2	3-Input NOR Circuit Truth Table	4-11
4-3	Variable Gain Operational Amplifier Characteristics	4-16
4-4	Gain Control Logic Truth Table	4-23
5-1	Test Equipment Required for Performance Verification	5-1
5-2	Power Supply Checks and Adjustments	5-5

CHAPTER I

GENERAL

1-1. INTRODUCTION

1-2. This Instruction Manual is for the AILTECH 7360 and AILTECH 7370 System Noise Monitors (SNM), Figure 1-1, and contains physical and functional descriptions, installation and inspection procedures, operating and maintenance instructions, and a parts list for each model. All schematics, electrical and assembly drawings are included, as are appendices for the available optional features. Unless otherwise stated, the information provided herein applies to both models.

1-3. GENERAL DESCRIPTION

1-4. The System Noise Monitors described in this Instruction Manual (7360 and 7370) are functionally identical. Each provides a readout of the Noise Figure of a unit under test (UUT) when connected in a valid measurement setup. The minimum test setup consists of a SNM, the UUT, and a solid state noise source of the AILTECH 7600 series.

1-5. The 7360 and 7370 SNM's are referred to as digital units because the readout is by three-digit LED display. AILTECH also manufactures the 7310 and 7320 which indicate Noise Figure by means of a front panel meter with two ranges. These are generally referred to as analog units.

1-6. The 7360 (Figure 1-2) is 7½ inches wide and is intended for bench-top use while the 7370 (Figure 1-3) is approximately 17 inches wide and is intended for rack mounting. The optional Rack Mount Angle Brackets (Option 11) must be attached for mounting in a standard 19 inch rack.

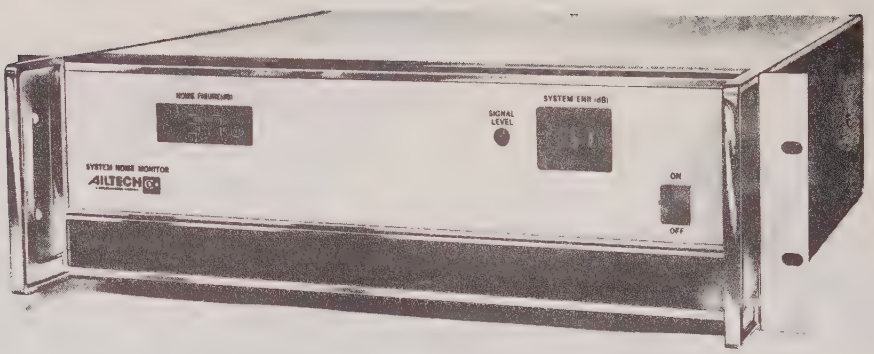
1-7. SAFETY PRECAUTIONS

1-8. The SNM's are low power instruments but when a unit is opened for service, there is the possibility of contacting the A.C. line. The potential hazard is reduced by covering all exposed contact points with insulating material. These instruments should be serviced by technically qualified personnel only.

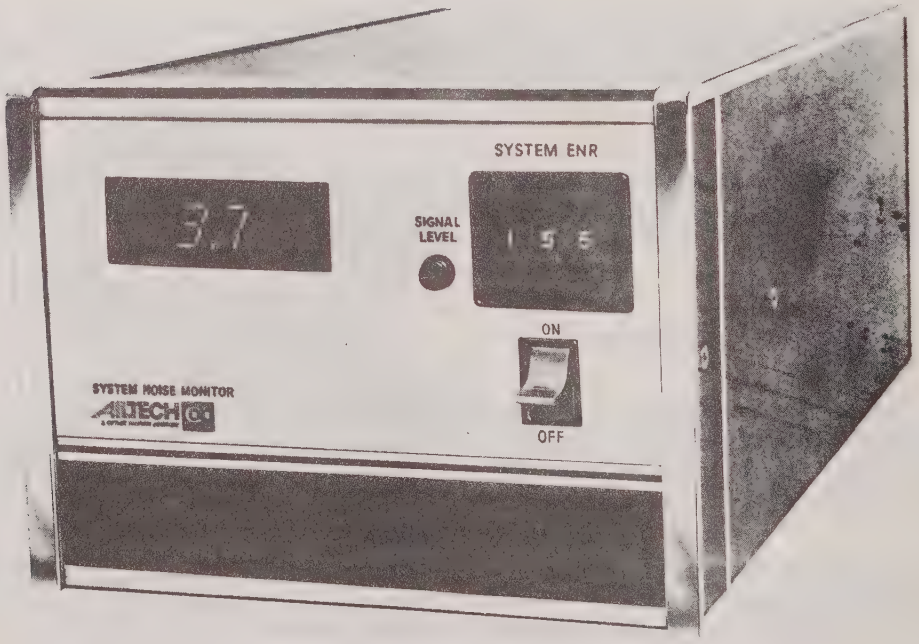
1-9. A standard three-wire, polarized line cord is supplied with the instrument and mates with an internationally accepted EMI/RFI line filter. The connector complies with all current and proposed domestic and international requirements for commercial test equipment.

1-10. TECHNICAL SPECIFICATIONS

1-11. A listing of technical specifications is provided in Table 1-1. Outline illustrations for both models are presented in Figure 1-2 and 1-3.



a) AILTECH 7370
(Shown with optional (-11)
rack mounting brackets)



b) AILTECH 7360

Figure 1-1. Digital System Noise Monitors

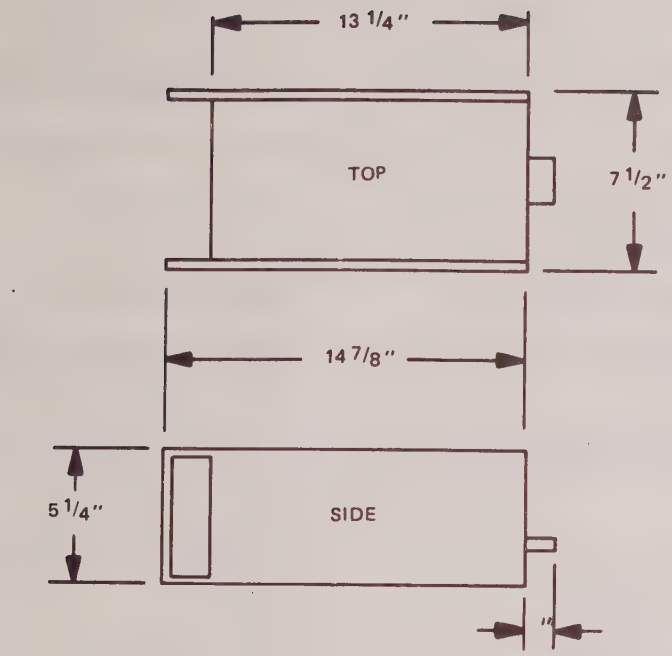


Figure 1-2. SNM, Model 7360 Outline Dimensions

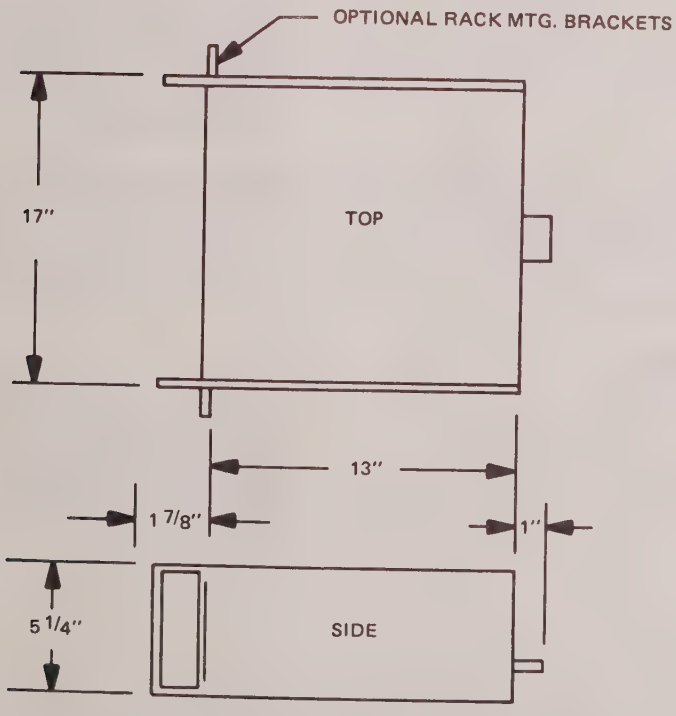


Figure 1-3. SNM, Model 7370 Outline Dimensions

TABLE 1-1. TECHNICAL SPECIFICATIONS

Input Frequency	10.7, 21.4, 30, 36, 45, 60 or 70 MHz (to be specified at time of order)
Bandwidth	10% of center frequency (nominal)
Minimum Operating Level (Note 1)	Less than -70 dBm
Signal Level Range (Note 2)	40 dB (minimum)
Input Impedance	50 ohms (nominal); 75 ohms, optional if specified at time of order.
Accuracy (Note 3)	0 to 6 dB: ±0.25 dB
	6 to 12 dB: ±0.5 dB
Measurement Range	0 to 19.9 dB
Excess Noise Ratio Calibration Range	6 to 15.9 dB
Noise Generator Power	Sufficient to drive all AILTECH Series 76 Solid-State Noise Sources
Recorder Output	7.5 volts across 1K ohms nominal for 0 dB indication
Auxiliary Output Connector (Recorder, Signal Monitor and All Options)	Amphenol 57-20240-1, mates with Amphenol 57-30240 supplied with unit (see para. 1-17).
Input Power	115/230 VAC ±15%, 50-400 Hz, 10 Watts
Dimensions	
7310	5 1/4"H × 7 7/16"W × 13 1/4"D (less handles) (13.3 × 18.9 × 34.3 cm)
7320	5 1/4"H × 17"W × 13 1/4"D (less handles) (13.3 × 43.2 × 34.3 cm) See Figures 1-2 and 1-3.

TABLE 1-1. TECHNICAL SPECIFICATIONS (continued)

Weight	
7360	10 lbs. Net (4.5 kg) 14 lbs. Shipped (6.3 kg)
7370	15 lbs. Net (6.8 kg) 19 lbs. Shipped (8.6 kg)

NOTES:

1. Lowest noise input level (noise source off), at which valid automatic measurements may be performed.

2. Range of noise levels (including Y-factor) over which valid measurements may be performed.

3. Accuracy in the automatic mode is defined as the maximum permissible deviation from a manual measurement made under the same conditions.

1-12. FUNCTIONAL DESCRIPTION

1-13. General

1-14. The System Noise Monitors are designed for both field and production applications where simplicity and high accuracy instrumentation are required. The SNM's are capable of providing fully automatic testing via a continuous indication of noise performance for a variety of components, assemblies and receivers. Simplified functional operation of the SNM's is described in the typical applications presented in the following paragraphs; a detailed functional description is provided in Section IV. All AILTECH solid state noise sources from 10 MHz to 18 GHz are usable with the SNM's described herein (see paragraph 1-22).

1-15. The System Noise Monitor in a Typical Application

1-16. In a typical measurement set-up for transistors, amplifiers, mixers, receivers, etc. such as that shown in Figure 1-4, the SNM furnishes modulated low level DC power to the noise source, which in turn provides alternating noise-on and noise-off periods to the unit under test (UUT).

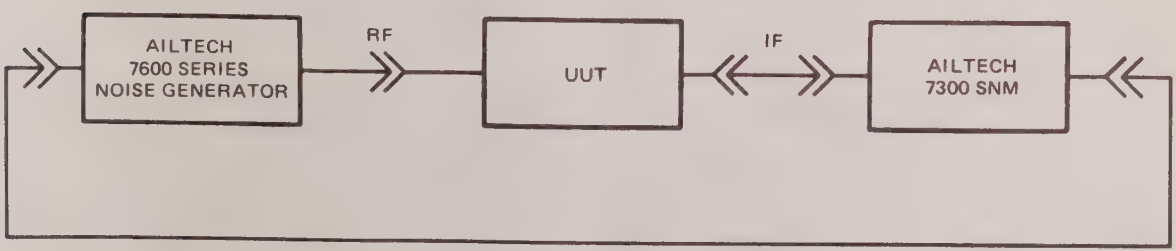


Figure 1-4. Typical Noise Figure Measurement Set-up Using the AILTECH 7300 System Noise Monitors

An intermediate frequency (IF) is derived either internal to the UUT in the case of a complete transceiver or externally by means of added downconverters. This signal, which consists of periods of IF noise from the UUT alone, alternating with periods of UUT noise plus that added by the noise source, is applied to the SNM input. The difference between the two detected levels derived from the IF signal is related to the noise performance of the UUT. This difference is synchronously detected and displayed directly as noise figure by the SNM.

1-17. AUXILIARY OUTPUTS

1-18. Several auxiliary outputs for remote monitoring or record keeping are available at J1, a multipin connector on the rear panel. The layout of J1 is shown in Figure 1-5. The outputs available are as follows:

a. Alarm Relay. An optional (Option 03) variable threshold alarm relay, applicable to all models.

b. Signal Monitor. A DC signal that varies from 0 to 6 volts (nominal) as the input IF level increases from the sensitivity limit to 50 dB above that limit. This is a non-linear output intended only to indicate signal level.

c. External Meter. A meter with 100 microamps full-scale sensitivity connected across pins 6 and 7 of J1 will track the excursion of the SNM front-panel indication. When Option 12, 10 volt recorder output, is installed the External Meter Function is not available.

d. Recorder Output. Approximately 7.5 volts into 1 K ohm for 0 dB Noise Figure indication.

e. Digital Output. The measured noise figure is available in BCD parallel format at pins 16 through 24 of J1. The levels are TTL compatible (positive true), and a strobe is provided to mark the end of each conversion cycle of the internal A/D converter. The strobe is a 5 volt positive pulse, 500 microseconds wide, occurring about every 16 milliseconds. The output data is updated during the pulse and is latched in between pulses.

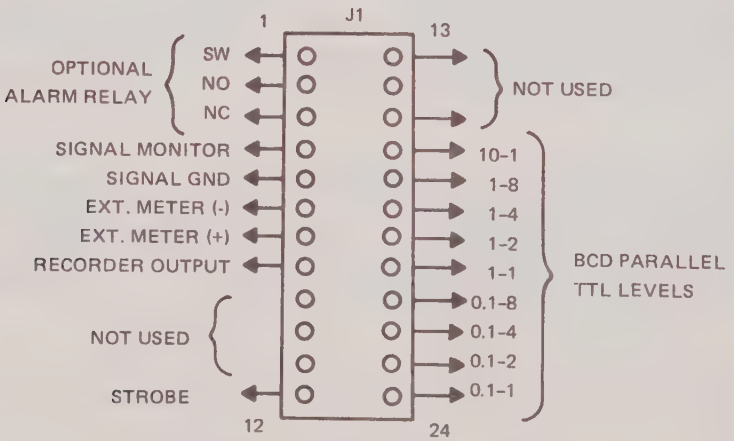


Figure 1-5. Layout of J1

1-19. OPTIONS

1-20. The following options are available for the 7300 System Noise Monitors and are listed here for reference and identification purposes. See the referenced appendices or documents for complete options descriptions.

a. Option 02, Radar Noise Monitor. Applicable to the 7370 SNM only. Provides for continuous, on-line, noise performance monitoring of an operating radar without interfering with the radar operation. Option 02 is covered in a separate manual.

b. Option 03, Alarm Indication. Applicable to both models. SPDT relay deenergizes when the measured noise figure degrades beyond a preset limit. The threshold is continuously variable from inside the unit. The relay contacts are available at J1 (see Figure 1-5). Refer to Appendix B.

c. Option 06, Special Paint. Applicable to both models. Front panels can be painted in accordance to customer's specifications (with customer supplied paint).

d. Option 07, High Sensitivity. Applicable to the 7370 SNM only. Improves the sensitivity to -100 dBm. Refer to Appendix C.

e. Option 09, Broadband Mixer Input. Available on 7370 SNM only. Addition of a broadband mixer with all ports (RF, LO, IF) available at the rear panel. The mixer cover 10 to 1,000 MHz. Refer to Appendix D.

f. Option 10, Front Panel Controls for Manual Operation. Applicable to both models. The controls required for manual Y-factor measurement are moved to the front panel. Refer to Appendix E.

g. Option 11, Rack Adaptor Brackets. Applicable to the 7370 SNM only. Permits mating the front panel with a standard 19 inch rack. See Appendix F.

1-21. ACCESSORIES

1-22. Noise Generators. A complete measurement setup requires a noise generator in addition to the SNM. All 7300 SNM's are designed to operate with solid-state noise sources of the 7600 series. Table 1-2 lists the applicable sources and Figure 1-6 illustrates some typical noise generators.

TABLE 1-2. APPLICABLE NOISE SOURCES

Part Number	07615	07616	07617	7650-X (1)	7660-X (1)
Frequency Range (GHz)	0.01-1.5	1-12.4	12.4-18	(2)	(2)
Excess Noise Ratio (dB)	15.5±0.5	15.5±0.5	15.5±1	see figure 1-7	see figure 1-7
Calibration Freq. (GHz)	0.03, 0.3, 1.0, 1.5	1,2,3.95, 8.2, 12.4	12.4,15,18,	3 points specified at time of order	
ENR Accuracy (3) (dB)	±0.3	±0.3	±0.25	±0.5(4)	±0.5(4)
VSWR (maximum)	1.2	1.2	1.3	4:1	4:1
Output Connector	N male	N male	OSM female	Type N-male	OSM-female

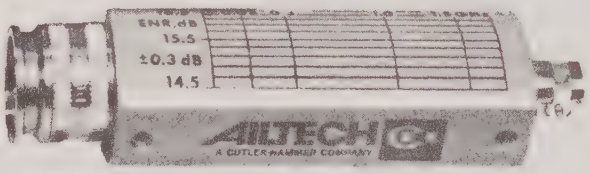
Table continued on page 1-8

TABLE 1-2. APPLICABLE NOISE SOURCES (Continued)

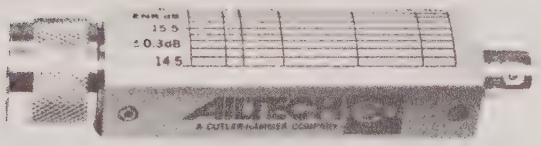
Part Number	07615	07616	07617	7650-X (1)	7660-X (1)
Input Connector	BNC female	BNC female	BNC female	BNC female	BNC female
Input Requirements	28 volts at less than 30 mA	28 volts at less than 30 mA	28 volts at less than 30 mA	28.0 V at 30 mA maximum	28.0 V at 30 mA maximum

NOTES:

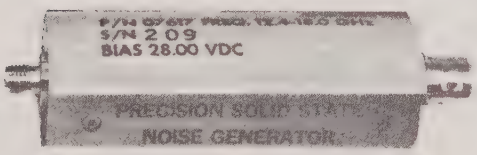
1. Last digit assigned to each specific noise source at time of order.
2. Up to 15% of the center frequency from 10 MHz to 18 GHz — wider bandwidths available.
3. Accuracy of the ENR data supplied at the calibration frequencies.
4. Higher accuracy available.



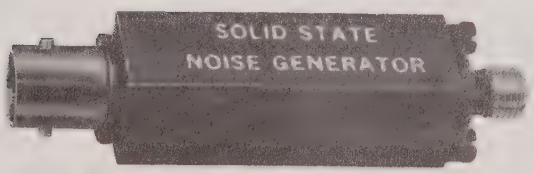
a) 07615 10 to 1500 MHz



b) 07616 1 to 12.4 GHz



c) 07617 12.4 to 18 GHz



d) 07660 Typical High Level System Noise Source

Figure 1-6. Typical Noise Sources Used With the 7300 SNM's

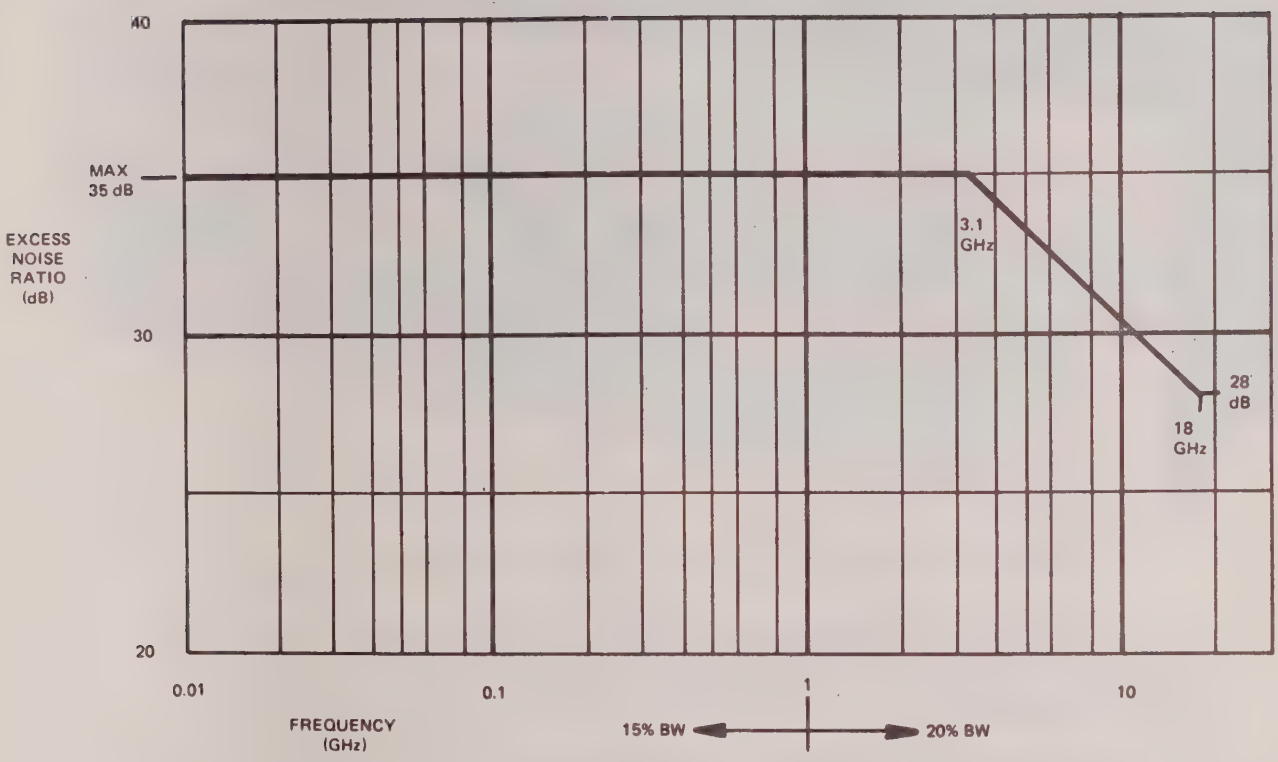


Figure 1-7. 7650/7660 Maximum ENR vs Frequency

1-23. Precision Attenuation. The AILTECH 32 Series Precision Attenuators are tuned, continuously variable attenuators which provide an accurate means of measuring Y-factor. These instruments are necessary for routine, periodic recalibration of the 7300 System Noise Monitors. However, for critical applications where it is desired to improve precision by recalibrating on-line on a short term basis, the Precision Attenuator becomes a valuable adjunct to the measurement setup. These attentuators (see Figure 1-8) are available at common intermediate frequencies in rack mount, cased, and unmounted configurations.

Figure 1-8. AILTECH 32 Precision Attenuator (Cased Version)

1-24. TEST EQUIPMENT

1-25. Table 1-3 lists the test equipment recommended for use in testing, adjusting and servicing SNM's.

TABLE 1-3. RECOMMENDED TEST EQUIPMENT

Description	Specification	Recommended Model
Precision Attenuator	IF equal to 7300	AILTECH 32 Series
Signal Generator	Calibrated output from -100 to -30 dBm at 7300 IF	Boonton 512
Digital Multimeter	4½ digits	Systron-Donner 7004A
Vector Voltmeter	10 to 100 MHz	PRD 2020
Oscilloscope	200 MHz 3 dB BW	Tektronix 475
Noise Generator	Compatible with UUT and SNM	AILTECH 76 Series
Amplifier	Compatible with Noise Generator and SNM	(Simulates UUT).

CHAPTER II

INSTALLATION

2-1. INTRODUCTION

2-2. This chapter describes unpacking, inspection, preparation for use and initial checkout of the AILTECH 7300 Series System Noise Monitors.

2-3. UNPACKING, INSPECTION AND DAMAGE CLAIMS

2-4. No special instructions or precautions are necessary for unpacking the SNM; the instrument is ready for use immediately upon receipt. The following checks should be made to assure that no damage has occurred during shipment.

a. Inspect the shipping container prior to acceptance from the carrier. Note any damage to the shipping container on the carrier's receipt.

b. Inspect the instrument for damage. Check for dents, scratches, broken switches, connectors, etc.

c. Remove the top and bottom covers and inspect for broken components or loose hardware.

d. If damage is not apparent until after the instrument has been accepted, file a claim for concealed damage with the carrier within 15 days after receipt. All packaging material must be kept for inspection by the carrier's agent. A copy of the claim must be forwarded to AILTECH.

2-5. ANCILLARY ITEMS

2-6. Each SNM is accompanied by a mating line cord, a mating plug for the auxiliary output connector, and one instruction manual. Before discarding the shipping container, make certain these items are removed.

2-7. RACK MOUNTING

2-8. Rack Mounting Adapter Kit, Option 11 is required to secure the AILTECH 7370 in a standard 19 inch rack. The kit consists of two right angle brackets which bolt to the side of the unit. Complete assembly instructions are provided with the kit.

2-9. PREPARATION FOR USE

2-10. Prior to shipment from the factory, the internal mode switches of the System Noise Monitor are set for normal automatic noise figure (or temperature) measurements, and the line voltage switch on the rear panel is set to the value appropriate for the shipping destination. However, it is good practice to check these settings prior to operating the instrument as follows:

a. Note the setting of the rear panel line voltage switch. Set it to 115 or 230 volts AC as required (see Figure 3-1).

b. Check both line fuses, F1 and F2, and make certain they are the correct value for the line voltage selected:

230 VAC: F1, F2 = 1/8 Amp.

115 VAC: F1, F2 = 1/4 Amp.

c. Remove the single Phillips-head screw holding the top cover in place, and remove the top cover.

d. See Figure 3-5 for the location of the IF-Video board and for the locations of the MAN-AUTO and noise generator ON-OFF switches on the IF-Video board.

e. Make certain that the MAN-AUTO switch is in the AUTO position and the noise generator ON-OFF switch is in the OFF position.

2-11. INITIAL CHECKOUT

2-12. This operational checkout is a preliminary test and is not intended to validate performance standards. (For complete Validation Procedure, refer to Chapter V.) Figure 3-1 and Table 3-1 locate and describe the function of the controls, indicators and connectors referenced below.

2-13. The equipment required for initial operational checkout is as follows:

a. Oscilloscope — Tektronix 475 (or equivalent).

b. Signal Generator — Boonton Model 102A (or equivalent).

c. Digital Multimeter — Syston Donner 7004A.

2-14. General

2-15. Perform the procedures detailed under paragraph 2-10. Connect the line cord to the appropriate AC power source.

CAUTION

The 7300 System Noise Monitors are low power instruments, but routine precautions should be observed due to the possibility of contact with the applied AC line.

2-16. Checkout Procedures

a. Set the power ON-OFF switch to the ON position, allow a few minutes for stabilization, and note that:

1. The red LED NOISE FIGURE DISPLAY indicates 19.9 dB.

2. The green SIGNAL LEVEL indicator is not illuminated.

b. Connect the output of the signal generator to the IF input. Set the output frequency to the center frequency of the SNM. Set the output level to rated sensitivity of the SNM:

-70 dBm for standard units

-100 dBm for units equipped with Option -07, High Sensitivity.

Note that the green SIGNAL LEVEL lamp is illuminated.

c. Locate the MAN-AUTO switch on the IF-Video board and set it to the MAN position. Note that the green SIGNAL LEVEL lamp extinguishes.

d. Connect the multimeter, set up to read +28 volts DC, to the BNC connector on the rear panel marked NOISE SOURCE. Not that the multimeter reads 0 ± 0.5 volts.

e. Set the noise generator ON-OFF switch on the IF video board to ON. Note that the multimeter reads +28.00 ±0.05 volts.

f. Disconnect the multimeter. Set the noise generator ON-OFF and MAN-AUTO switches on the IF-Video board to OFF and AUTO respectively. Connect the oscilloscope to the NOISE SOURCE BNC connector on the rear panel. Note that the output is a rectangular, positive pulse, alternating between 0 and +28 volts, at about a 550 Hz rate).

g. Disconnect the oscilloscope, and replace the top cover.

NOTE

If the instrument fails any portion of the checkout procedure, it requires adjustment or repair. Refer to Chapter V for adjustment and troubleshooting instructions. If the unit is still under warranty, contact your local AILTECH representative.

CHAPTER III

OPERATING INSTRUCTIONS

3-1. GENERAL

3-2. This chapter provides a description of the SNM operating controls, indicators and connectors and typical SNM operating procedures.

3-3. DESCRIPTION OF OPERATING CONTROLS, INDICATORS AND CONNECTORS.

3-4. The front and rear panel controls, indicators and connectors for SNM Models 7360/7370 are listed in Table 3-1 and illustrated in Figure 3-1. The functions of the controls, indicators and connectors for Models 7310 and 7320 are identical.

3-5. SET-UP PROCEDURES

3-6. The AILTECH 7300 System Noise Monitors are normally applied to the continuous or periodic measurement of a single receiving system, or repeated measurements of similar types of devices (as on a production line test station). Therefore, some care should be exercised in setting up the measurement system to insure the validity of the indicated results.

3-7. There are three major factors to be considered in setting up the measurement system:

a. Interconnections.

b. Establishment of the correct Excess Noise Ratio (ENR) setting for the front panel thumbwheel switch on the SNM.

c. Establishment of signal levels within the measurement range of the SNM.

3-8. Interconnections

3-9. In general, there are two types of set-ups for noise parameter measurements. For purposes of identification these will be referred to as "bench" and "operating" noise measurements.

3-10. Most true noise figure measurement are of the bench type. In this case, the setup will be as indicated in Figure 3-2.

3-11. If the noise source is a typical laboratory noise generator with an excess noise ratio (ENR) less than 16 dB — such as the AILTECH 7615, 7616, and 7617 Noise Generators — it can be connected directly to the input of the unit-under-test (UUT).

3-12. If the noise source is a high-level unit with an ENR greater than 16 dB — such as most units in the 7650, 7660 series — a calibrated attenuator sufficient to reduce the ENR to a value between 6 and 15.9 dB must be inserted between the noise source and the input of the UUT (effective ENR is the noise source ENR less the attenuation in dB).

3-13. Operating measurements are those made with the receiver connected in its normal operating environment. In most cases, this means the input connected to an antenna. Noise is injected into the system by means of a directional coupler (see Figure 3-3). This setup usually requires a high level noise source, such as the AILTECH 7650 or 7660.

TABLE 3-1. AILTECH 7360/7370 SYSTEM NOISE MONITORS CONTROLS, INDICATORS AND CONNECTORS

Key (Figure 3-1)	Title	Reference Designation	Function
1	ON-OFF	S1	Lever switch controls application of AC power.
2	SYSTEM ENR (dB)	S3	Thumbwheel switch calibrates SNM for selected excess noise ratio.
3	SIGNAL LEVEL	DL2	Green indicator is illuminated when the input IF level exceeds some arbitrary minimum.
4	NOISE FIGURE (dB)	—	Three digit LED display indicates Noise Figure.
5	Fuse	F1	Line fuse.
6	Fuse	F2	Line fuse.
7	LINE	S11	Slide switch selects primary AC input line voltage.
8	AC INPUT	—	Recessed plug for application of primary AC input.
9	Connector	J1	Multipin connector (Amphenol 57-20240-1, mate supplied) for auxiliary outputs (see paragraph 1-17).
10	DISPLAY TEST	S8	Momentary pushbutton tests LED display
11	IF INPUT	J8	BNC female connector for application of IF signal from unit under test.
12	NOISE SOURCE	J9	BNC female connector provides excitation for the AILTECH Series 7600 Noise Source.

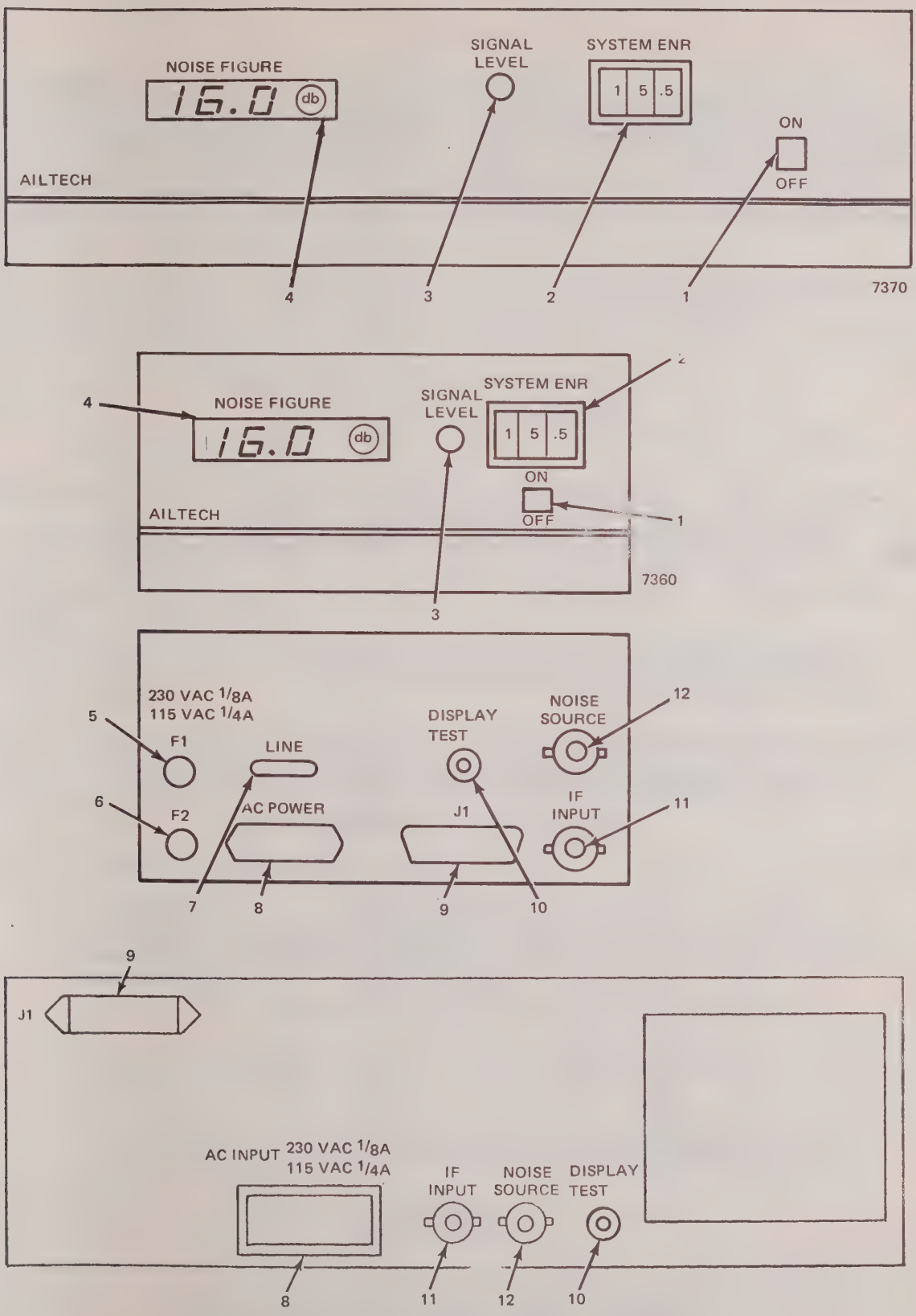
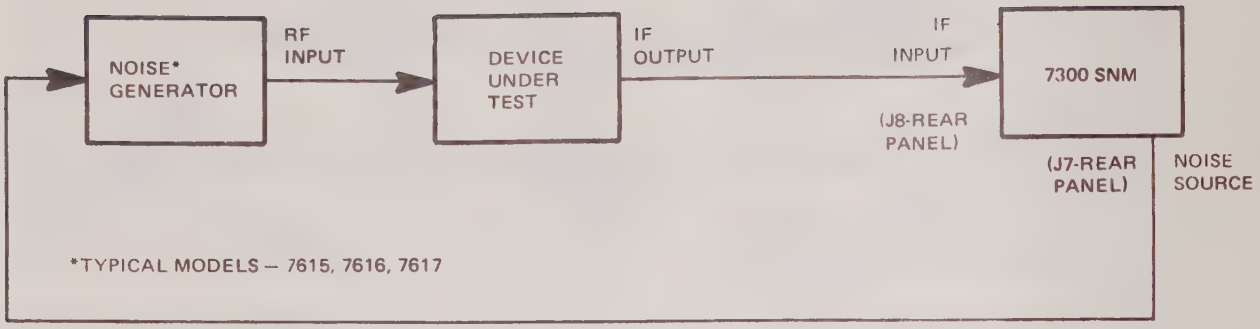
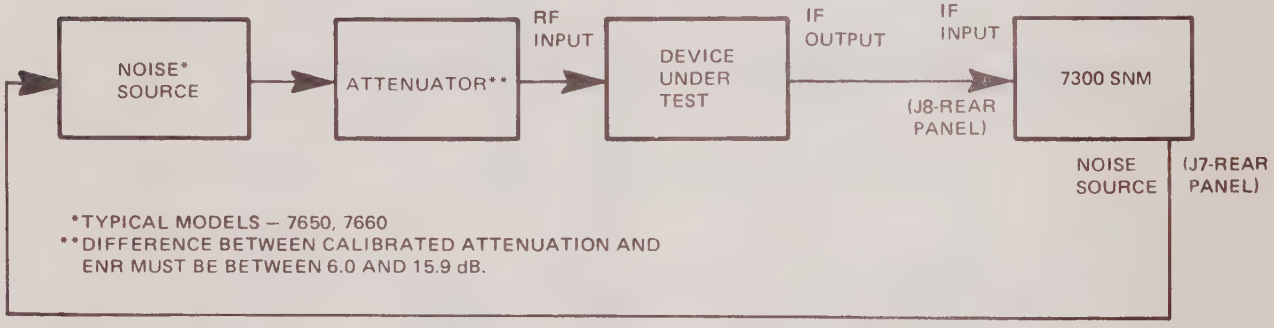


Figure 3-1. 7360/7370 SNM Control, Indicator, Connector Locations



(a) Set-up for Bench Measurements Using Noise Sources With ENR's Between 6.0 and 15.9 dB



(b) Set-up for Bench Measurements Using High-Level Noise Sources

Figure 3-2. Bench Measurement Set-ups

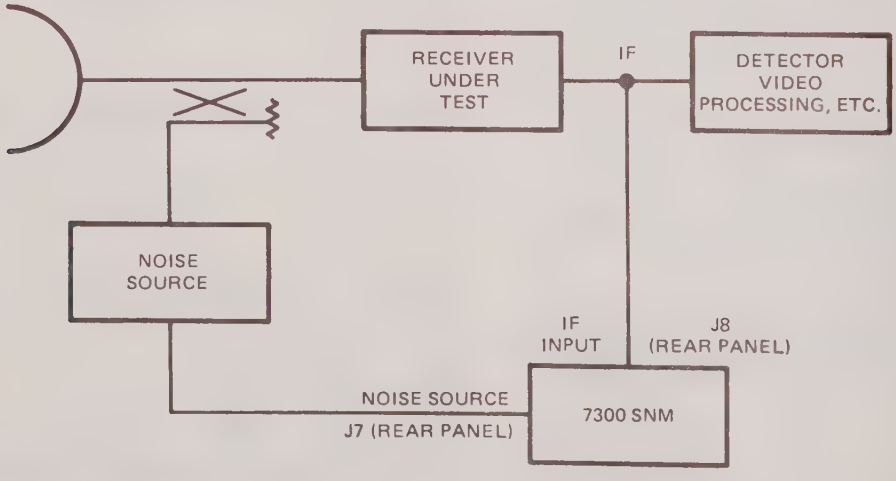


Figure 3-3. Typical "Operating" Measurement Set-up

3-14. The measurement performed by a setup such as that illustrated in Figure 3-3 is often called Operating Noise Figure. This is a noise figure measurement in which the cold noise temperature is that of the actual operating termination, but the results are displayed as though the termination was at the standard reference temperature, 290 kelvins. In general, this measurement will yield lower noise figure readings than a true noise figure measurement (assuming a quality antenna with an effective noise temperature less than 290K). This type of measurement is quite commonly made on radar receivers, and is sometimes called radar noise figure.

3-15. If the SNM readout is in noise temperature, then the measured parameter is Operating Noise Temperature. This parameter is often measured on high-sensitivity, long range receivers, such as satellite earth stations.

3-16. Other factors to be considered are:

a. Frequency compatibility between the noise source and the RF input of the UUT (a matter of proper noise source selection).

b. Frequency compatibility between the IF output of the UUT and the System Noise Monitor. This may require frequency conversion (see paragraph 1-19 for options which provide this feature).

3-17. Excess Noise Ratio Setting

3-18. The accuracy of the 7300 SNM depends upon accurate setting of the front panel ENR thumbwheel switch. Any error in this switch setting is translated directly — dB for dB — to the noise figure indication.

3-19. Laboratory or bench-type noise generators such as the AILTECH 7615, 7616, and 7617 (see Figure 1-6) have an ENR vs. frequency calibration chart attached or printed on the generator body and are accompanied by a record of calibration. System noise sources, such as the 7650 and 7660 are also accompanied by calibration records.

3-20. To determine the ENR thumbwheel settings:

a. Locate the two frequencies on the noise source calibration record (or calibration chart) that straddle the RF input frequency of the UUT (assuming the input frequency does not coincide with a calibration point).

b. Use straight line interpolation to determine the basic noise source ENR.

c. If the set-up is as shown in Figure 3-2(a), adjust the ENR thumbwheel to the result in (b) to the nearest 0.1 dB.

d. If the set-up is as shown in Figure 3-2(b), subtract the attenuation (in dB) from the ENR determined in (b). Adjust the ENR thumbwheel to the resulting difference to the nearest 0.1 dB.

3-21. Establishing the Correct Signal Levels

3-22. The basic sensitivity (low point of the valid signal level range) of the 7300 System Noise Monitors is better than -70 dBm. This is not the point at which the green Signal Level light comes on. This light is meant only as a gross indication that some signal is available from the UUT.

3-23. To determine sensitivity or low end of the signal level range a signal generator to provide low level signals at the SNM center frequency is required (a typical unit is the Boonton 102A).

a. Make certain the SNM is in the AUTO mode (S101).

b. Connect a signal generator tuned to the center frequency of the SNM to the IF Input.

c. Gradually increase the signal generator output level from about -85 dBm until the green Signal Level light illuminates. Note the generator output level.

d. Increase the generator output 5 dB above the point where the Signal Level light comes on. This is the sensitivity or lower end of the valid signal level range. Note that this level is less than -70 dBm, and record it for future reference.

NOTE

If a continuous indication of signal level is desired, see Paragraph 3-33.

3-24. The upper end of the valid signal level range will be 40 dB above the sensitivity as determined from paragraph 3-23 (d). All signals — both with the noise source on and the noise source off — must remain within this range. Figure 3-4 illustrates this range using typical levels.

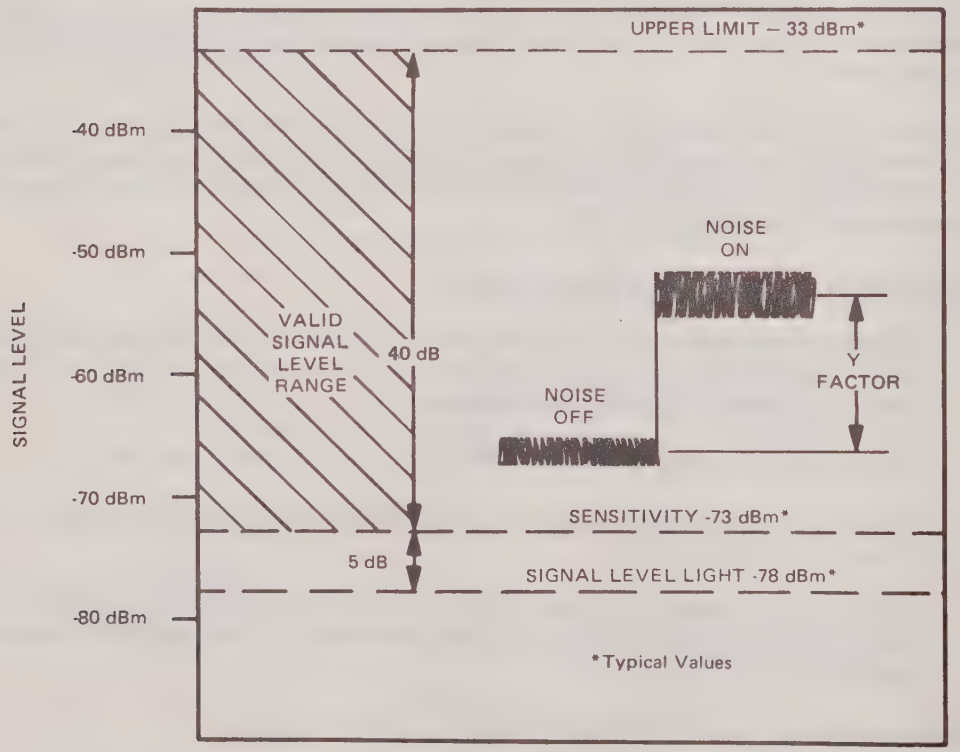


Figure 3-4. Illustration of Sensitivity and Signal Level Range

3-25. To insure that the UUT output is within the valid range, proceed as follows:

a. Remove the top cover of the SNM and locate the following controls on the IF-Video board (see Figure 3-5). These controls are on the front panel of those units equipped with Option 10, Manual Front Panel Controls:

MAN-AUTO switch, S101

MANUAL GAIN control, R140

Noise Generator ON-OFF Switch, S102

b. Connect a signal generator tuned to the SNM center frequency and set the output level as described in paragraph 3-23 (d).

c. Set the following controls as indicated:

1. MAN-AUTO switch S101 to MAN

2. Noise Generator switch S102 to OFF

d. Adjust manual GAIN control, R140, for a convenient noise figure reading (about 6 dB). Record the setting.

e. Without disturbing the preceding settings, disconnect the signal generator and set up the measurement system in accordance with Figure 3-2 or 3-3 as required.

f. If the noise figure indication with the control settings as above is higher than (d), additional gain is required between the UUT and the SNM input. Add gain as required (or see paragraph 1-19 for an option to provide better sensitivity) to bring the reading lower in noise figure than (d) and proceed to (h).

g. If the indication is a lower noise figure than (d), set Noise Generator switch S102 to ON.

h. Add attenuation at the SNM input until the indication returns to (d). If the total attenuation required is greater than 40 dB, there is too much gain in the UUT, and fixed attenuation must be provided at the SNM input as part of the set-up.

3-26. After establishing the correct input levels, set MAN-AUTO switch S101 to AUTO and Noise generator switch S102 to OFF. Replace the top cover.

3-27. OPERATION

3-28. Once set-up is accomplished, the ENR switch correctly set, and the correct signal levels established, the System Noise Monitor will automatically indicate noise figure. No further operator activity is required.

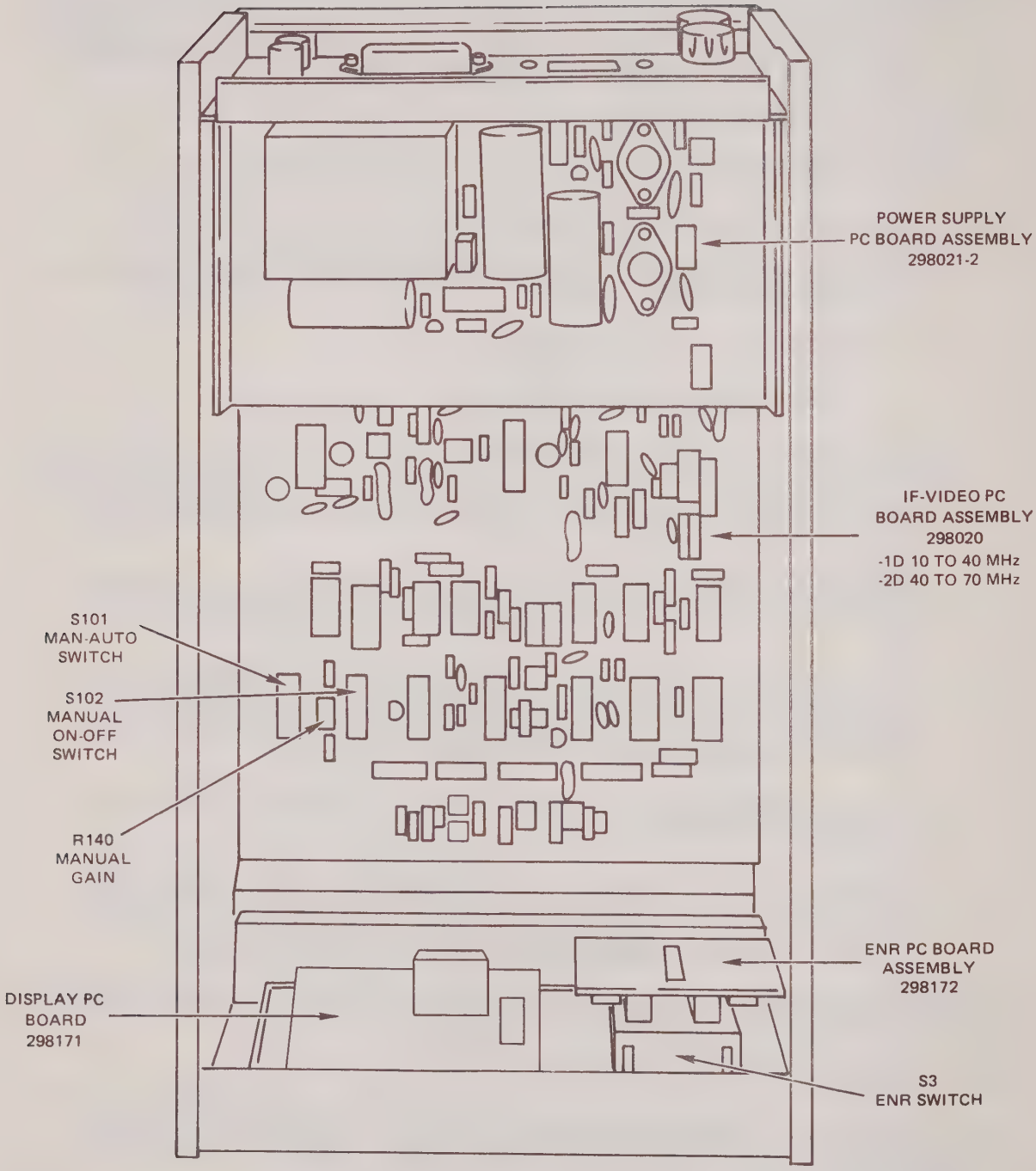


Figure 3-5. Location of the Manual-Auto Controls
(Digital PC Board P/N 298170, Removed for Illustration)

3-29. USE OF AUXILIARY OUTPUTS

3-30. Paragraph 1-17 briefly described several auxiliary outputs available at J1 on the rear panel. These outputs may be used for monitoring signal level, for permanent records of noise figure variations with time, and for providing a readout at a remote location (see Figure 1-5 for layout of J1).

3-31. Signal Monitor, J1, Pin 4. This output provides a DC signal that varies from near zero to approximately 6 volts as the input signal level increases by about 40 dB from the sensitivity limit. It is a non-linear, uncalibrated output; however, it can be very useful for insuring that the UUT output level remains in the valid range as established by paragraph 3-25. This can be accomplished as follows:

a. Connect a voltmeter, 0 to +10 volts DC capability between J1-4 (+) and J1-5 (-, GND).

b. Proceed as indicated in Paragraph 3-23.

c. Record the voltmeter indication upon completion of paragraph 3-23 (d) This indication corresponds to signal level at the low-limit of the valid range.

d. Increase the signal level by 40 dB, less the expected Y-factor (see paragraph 3-32). Record the voltmeter indication which represents the maximum permissible signal level.

3-32. When operating the SNM in the AUTO mode, the signal levels are valid as long as the voltmeter remains within the limits established in paragraph 3-31 (c) and (d).

NOTE

The expected Y-factor is a function of the noise figure of the UUT and the effective ENR. For noise figures less than 6 dB and ENR's greater than 14 dB, the expected Y-factor can be approximated by subtracting noise figure from ENR (both quantities in dB). For other situations it may be calculated from:

$$Y_{(dB)} = 10 \text{ Log } \left(\frac{ENR}{F} + 1 \right) \qquad (3-1)$$

where ENR and F are expressed as power ratios.

It may also be determined from the AILTECH Noise Figure Slide Rule, Figure 3-6, or the nomograph of Figure 3-7.

3-33. External Meter, J1, Pins 6 and 7. This feature provides for a readout of noise figure at a remote location. A meter connected across the referenced pins (+ to pin 7; - to pin 6) will track the noise figure excursions of the UUT. The equation governing the meter scale is:

$$F_{dB} = 10 \text{ Log } \frac{I_{fs}}{I_m} , \qquad (3-2)$$

where, I_{fs} = full-scale current

I_m = meter current corresponding to the indicated noise figure

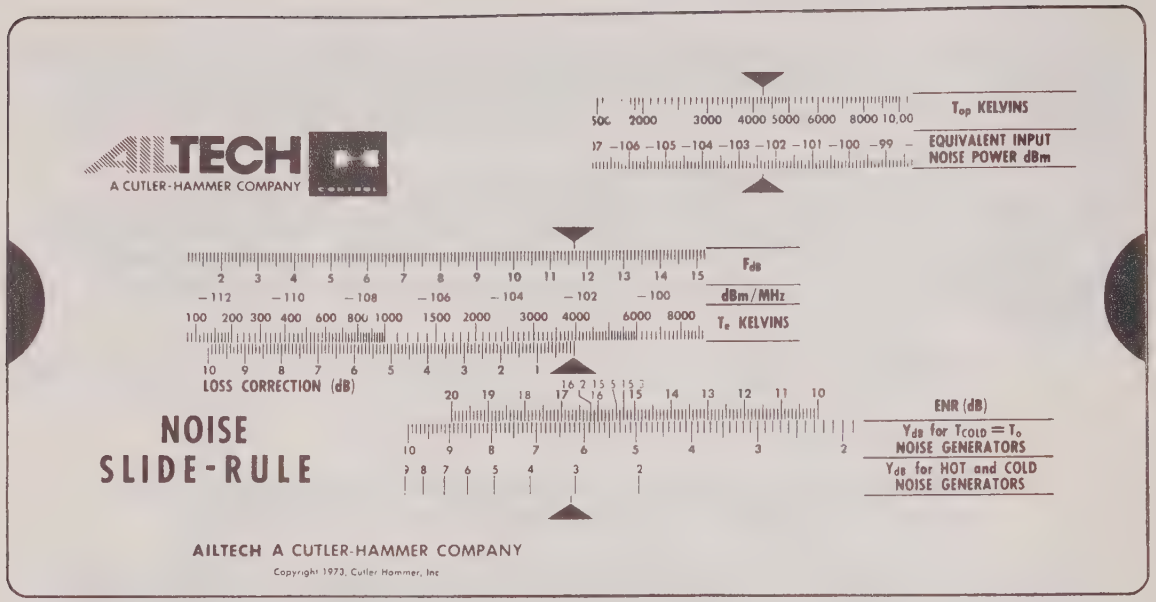


Figure 3-6. AILTECH Noise Figure Slide Rule

3-34. The external meter leads are ungrounded and should be twisted and shielded for runs of more than one foot.

3-35. Recorder Output, J1, Pin 8. This output is a voltage referenced to ground (pin 5) that tracks the meter excursions. It will provide approximately +7.5 volts across 1K ohm for 0 dB indication. This feature is necessary in evaluating noise performance excursions with time, investigating suspected intermittents in a receiver system, and providing hard copy for swept measurement systems.

3-36. The recording device will require calibration. This can be done in the Manual mode by applying a CW signal from a generator to the IF input, and marking the recorder position for various indications. This calibration will remain valid when the SNM is switched back to the Auto mode.

3-37. Digital Outputs, J1, pins 12 and 16 thru 24. Pins 16 thru 24 provide a digital output representing the indicated noise figure in BCD parallel format. Pin 12 is a strobe output that goes "High" during the conversion cycle, and "Low" when the data are valid and latched for display or readout (see Figure 3-8).

3-38. Figure 1-5 provides the overall layout for J1; however, for reference, the pins providing the BCD outputs are again identified in Table 3-2. The identifying notation is as follows: 1-4 indicates the "4" bit of the units digit. For purposes of illustration, Table 3-2 also includes the outputs for a typical noise figure indication of 7.3 dB.

TABLE 3-2. BCD OUTPUTS

J1 Pin No.	BCD VALUE	Output for 7.3 dB Noise Figure	
16	10-1	L	0
17	1-8	$\overline{L}$	7
18	1-4	H	
19	1-2	H	
20	1-1	H	
21	0.1-8	$\overline{L}$	3
22	0.1-4	L	
23	0.1-2	H	
24	0.1-1	H	

3-39. The BCD outputs from pins 16 thru 24 of J1 are TTL compatible, positive logic; thus, a "Low" is represented by 0 to +0.8 volts, and a "High" by approximately +3 to +5 volts.

3-40. MANUAL NOISE FIGURE (TEMPERATURE) MEASUREMENTS

3-41. All AILTECH 7300 Series System Noise Monitors include a manual mode of operation. In this mode, the noise source can be turned on or off under operator control (rather than automatically switched), and the internal automatic control circuits are disabled. The instrument then provides a relative, uncalibrated indication of input power level.

3-42. The major feature of the manual noise parameter measurement is improved accuracy. The measurement method utilizes a substitution technique that eliminates potential errors due to the direct reading accuracy of the SNM.

3-43. The measurement is more time-consuming and difficult than the automatic measurement described earlier, and it requires additional equipment; however, it does provide a convenient means of checking the performance of the SNM and calibrating the unit.

3-44. The set-ups are the same as those described earlier, except that a Precision IF Attenuator is inserted just prior to the SNM IF input; however, it may be necessary to insert additional gain due to the attenuator insertion loss. A typical attenuator suitable for this purpose is the AILTECH 32 Series (see Figure 1-8).

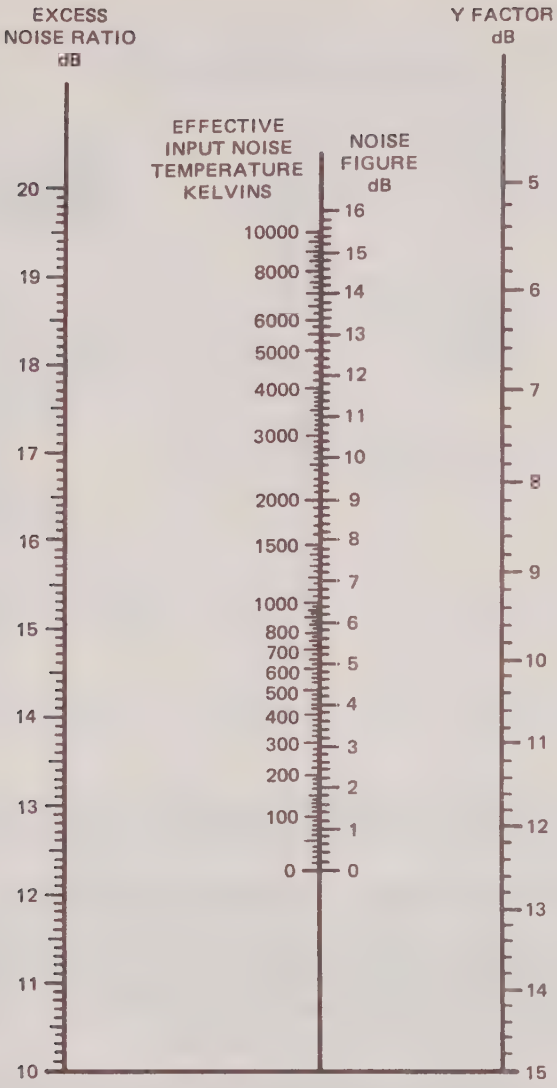


Figure 3-7. Nomograph for Determining Noise Figure or Temperature

3-45. The measurement procedure is as follows:

a. Remove the top cover and locate MAN-AUTO switch S101, Noise generator ON-OFF switch S102, and Manual GAIN control R140 on the IF-Video Board (see Figure 3-5).

b. Set MAN-AUTO switch S101 to MAN, and Noise Generator switch S102 to OFF.

c. Set the Precision Attenuator to 0 dB, and adjust the manual GAIN control, R140, for a convenient reference indication on the NOISE FIGURE display less than 19.9 dB (preferably about 6 dB). If the input signal level is too low to achieve this condition, the ENR thumbwheel switch may be set to a lower number. Note the indication.

d. Set Noise Generator ON-OFF switch S102 to ON. Note that the indication decreases (lower Noise Figure reading).

e. Increase the setting of the Precision Attenuator until the indication returns to the reference noted in (c). Record the attenuation change which is the Y-factor in dB.

f. Noise Figure or Operating Noise Temperature may be calculated from Equations 3-3.

$$F_{(dB)} = ENR_{(dB)} - 10 \text{ Log } (Y\text{-}1) \qquad (3\text{-}3a)$$

$$T_{op} = \frac{290\ (ENR)}{Y\text{-}1} \qquad (3\text{-}2b)$$

In both proceeding equations the ENR is the actual effective value after decoupling or attenuation (if any) — not the setting of the thumbwheel switch. Note also that ENR must be expressed as a power ratio for use in (b). Y-factor is also expressed as a power ratio in both equations.

3-46. The noise parameters may also be calculated using the AILTECH Noise Figure Slide Rule, Figure 3-6 or the nomograph of Figure 3-7.

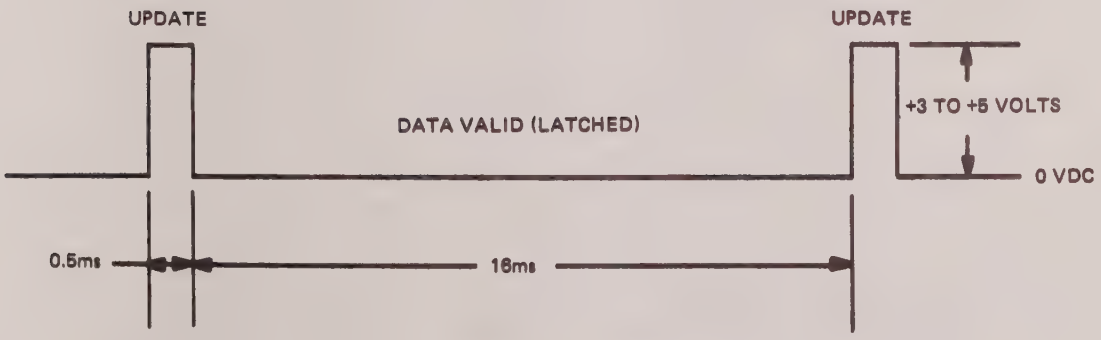


Figure 3-8. BCD Data Output Strobe

CHAPTER IV

THEORY OF OPERATION

4-1. INTRODUCTION

4-2. This chapter contains noise figure measurement general theory and associated mathematics, and an overall functional block diagram description of the SNM. Also included are detailed, individual circuit descriptions.

4-3. GENERAL THEORY

4-4. Noise Figure Theory

4-5. Noise Figure can be defined as the ratio of the noise power available at the output of a network, when the input termination is at the standard reference Temperature (T_o = 290K), to that which would be available at the output of an ideal noiseless network of otherwise identical characteristics. This can be expressed mathematically as:

$$F = \frac{N_o}{GN_i} \qquad (4\text{-}1)$$

where:

F = Noise Figure Ratio

N = Noise Power (i = input, o = output)

G = Gain of network

By rearranging equation 4-1,

$$N_o = N_i FG \qquad (4\text{-}2)$$

The noise power available at the input is that generated by the input termination and can be written as:

$$N_i = kT_oB \qquad (4\text{-}3)$$

where:

k = Boltzmann's constant = 1.38×10^{-23} joules/K

B = bandwidth in Hz

T_o = standard reference temperature (290K)

NOTE

All temperatures in these equations are expressed as absolute temperatures (Kelvins) and are related to the Centigrade (Celsius) scale as follows:

$$K = {}^{o}C + 273$$

Substituting in Equation 4-2,

$$N_o = kT_o BFG \tag{4-4}$$

Expansion of this relation yields:

$$N_o = \left[kT_oB + (F-1)kT_oB\right]G \tag{4-5}$$

Although Equation 4-5 expresses noise figure implicitly in terms of its effect on the network output, it is sometimes considered more basic than Equation 4-1 because:

- It can be used to show the effect of an input termination temperature differing from the reference temperature (T_o).
- It can be conveniently represented pictorially.
- It provides the basis for an indirect, but convenient method of measuring noise figure.

Figure 4-1 is a representation of Equation 4-5. Noise source A is the input termination while noise source B is a fictitious source representing network contribution to the noise output with reference to the input.

4-6. Noise Figure Measurement

4-7. Figure 4-1 can be modified as indicated in Figure 4-2. A switch has been added so that the original input termination (A) can be disconnected and the network input terminated in a second source (C) at temperature T_2 (the temperature of the noise generator).

The available output power of the network for this condition is:

$$N_o = \left[kT_2B + kT_oB\,(F-1)\right]G \tag{4-6}$$

Dividing Equation 4-6 by Equation 4-4 yields:

$$\frac{N_{o2}}{N_{o1}} = \frac{T_2 + T_o\,(F-1)}{T_oF} \tag{4-7}$$

Adding -1 to both sides of the equation and rearranging terms yields:

$$F = \frac{\left(\frac{T_2}{T_o} - 1\right)}{\left(\frac{N_{o2}}{N_{o1}} - 1\right)} \tag{4-8}$$

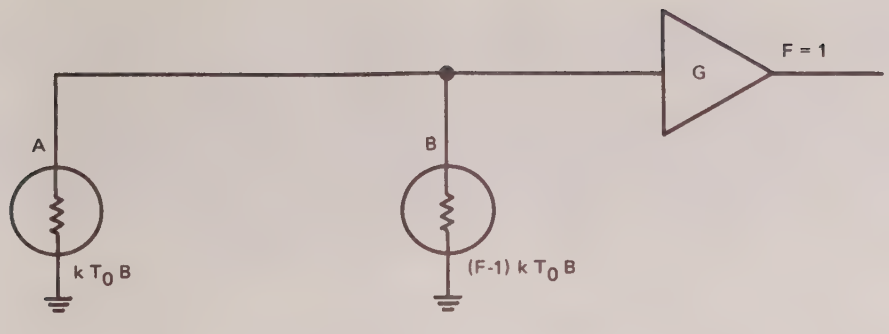


Figure 4-1. Equivalent Noise Representation of a Noisy Network

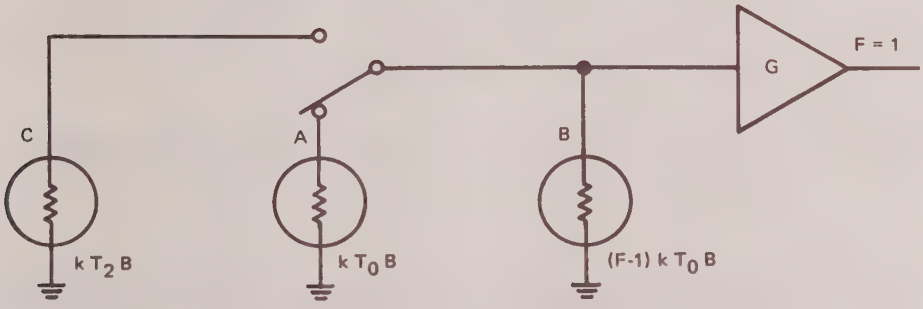


Figure 4-2. Equivalent Representation of Noise Figure Measurement Set-up

Equation 4-8 is the basic relation for determining noise figure. The numerator is called excess noise ratio and is usually expressed simply as ENR. It represents the relative increase in noise power at the network input when the switch is operated. If ENR is known, the ratio N_{o2}/N_{o1} (commonly called Y-factor) can be measured, and the noise figure computed from Equation 4-8. Note that it is not necessary to measure the absolute power levels at the network output, merely their ratio.

Therefore,

$$F = \frac{ENR}{Y\text{-}1} \qquad (4\text{-}9a)$$

or, expressed in dB,

$$F_{(dB)} = ENR_{(dB)} - 10 \text{ Log } (Y\text{-}1) \qquad (4\text{-}9b)$$

4-8. Operating Noise Figure and Temperature Measurement

4-9. In those applications where it is not possible to separate a standard termination from a termination with known ENR as in an operating radar system, a different measurement must be taken. Here, a front-end performance factor (operating noise figure or noise temperature) is measured. Since it is very difficult to separate system noise from the antenna or receiver input generated noise, the two are lumped together and measured. Figure 4-3 illustrates this technique.

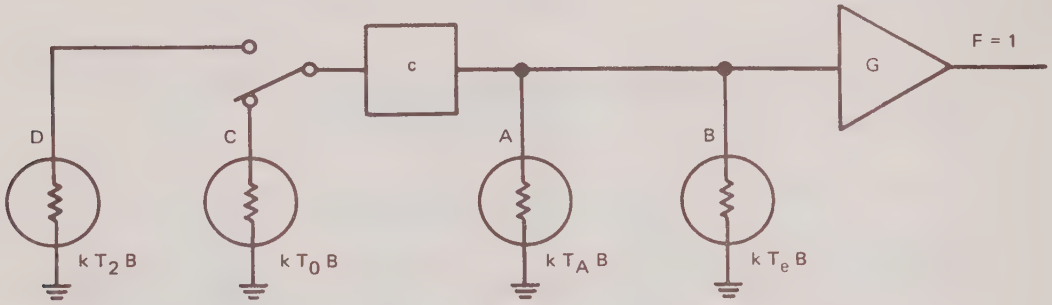


Figure 4-3. Equivalent Representation of an Operating Noise Measurement

4-10. The element marked "C" represents the directional coupler through which the noise is injected. T_e is the effective input noise temperature of the receiver and comparison with Figures 4-1 and 4-2 shows that it is related to noise figure by:

$$T_e = (F-1)\ T_o \qquad (4\text{-}10)$$

T_A (Figure 4-3) represents the effective antenna temperature. The available output noise power from the network under operating conditions is given by:

$$N_o = k(cT_o + T_a + T_e)BG \qquad (4\text{-}11)$$

When the reference noise source is energized (switch connected to D) the available output noise:

$$N_o = k(cT_2 + T_a + T_e)BG \qquad (4\text{-}12)$$

Dividing Equation 4-12 by Equation 4-11 yields:

$$\frac{N_{o2}}{N_{o1}} = \frac{cT_2 + T_a + T_e}{cT_o + T_a + T_e} \qquad (4\text{-}13)$$

Adding -1 to both sides of the equation and rearranging terms,

$$Y\text{-}1 = c(T_2 - T_o)/cT_o + T_a + T_e \qquad (4\text{-}14)$$

In Equation 4-14, the term cTo in the denominator represents the portion of noise coupled into the system from the noise source when it is deenergized. In most systems, the noise source is decoupled by at least 20 dB and therefore, the term represents an insignificant noise contribution and can be disregarded. Realizing that $(T_2-T_o)/T_o$ is the ENR of the reference noise source, $(T_a + T_e)$ is the operating noise temperature (T_{op}), and the operating noise figure (F_o) is $(T_a + T_e)/T_o$, terms in Equation 4-14 can be rearranged to obtain:

$$F_{op} = cENR/Y\text{-}1 \qquad (4\text{-}15a)$$

or

$$F_{op}\,(dB) = ENR_{(dB)} - c_{(dB)} - 10\,Log\,(Y\text{-}1) \qquad (4\text{-}15b)$$

This relation has the same basic form as Equation 4-9. The quantity cENR represents the power available from the system noise source at the receiver input.

Alternately,

$$T_{op} = \frac{cT_o\,(ENR)}{Y\text{-}1} \qquad (4\text{-}16)$$

4-11. FUNCTIONAL DESCRIPTION (AUTOMATIC NOISE MEASUREMENT)

4-12. The functional circuitry required to make a noise measurement is contained on the IF-Video Board while the Power Supply Board contains the regulated power supplies and the noise source modulator. The Digital P.C. Board converts the analog information to BCD format. See Figure 4-4 for an overall block diagram of the AILTECH System Noise Monitor.

4-13. A free-running multivibrator, operating at approximately 550 Hz modulates the DC power source for the Noise Generator, alternately energizing and deenergizing the unit. The resulting two noise levels are applied to the system under test. The IF output of the system will also be two levels of noise where the lower level represents the system noise when its input is normally terminated. The higher level is the system noise plus the generator noise. These signals are further amplified by the IF amplifier in the SNM and are then detected by a square law device providing two voltages proportional to the noise powers in the IF signal. A sample of this detected signal is supplied to an AGC amplifier that is gated to provide an output only during the time the noise generator is turned off. This output is used to control the gain of the IF amplifier, so that the noise-off signal is maintained at a constant level.

The above procedure may be described mathematically as follows:

The Noise-on voltage at the output of the square law detector is given by:

$$V_2 = pN_2 \qquad (4\text{-}17)$$

The Noise-off voltage by:

$$V_1 = pN_1 \qquad (4\text{-}18)$$

Where

p = constant

N_1, N_2 = Noise power available at the output of the UUT.

A synchronous integrator derives a D.C. voltage proportional to the difference between these two levels.

$$V_m = V_2 - V_1 \tag{4-19}$$

or

$$V_m = p(N_2 - N_1) \tag{4-20}$$

Rearranging terms

$$V_m = pN_1 \left(\frac{N_2}{N_1} - 1\right) \tag{4-21}$$

From the previous discussions:

$$\frac{N_2}{N_1} = Y \tag{4-22}$$

Therefore,

$$V_m = pN_1 (Y-1) \tag{4-23}$$

From Equation 4-9a

$$V_m = pN_1 \left(\frac{ENR}{F}\right) \tag{4-24}$$

Equation 4-24 indicates that, if ENR is known and N_1 is constant (a condition satisfied by the gated AGC amplifier), a voltage inversely proportional to the noise figure of the UUT is generated.

Also, from Equation 4-16:

$$Y-1 = \frac{cT_o(ENR)}{T_{op}} \tag{4-25}$$

and

$$V_m = pN_1 \frac{c(ENR)}{T_{op}} \tag{4-26}$$

4-14. The D.C. voltage is applied to the Digital Board. The signal is categorized as to range and converted to a binary signal by means of an auto-ranging analog to digital converter (ADC). The range signal and the binary information are utilized to address a read-only-memory (ROM). The ROM is a look-up table which outputs a parallel, 2-1/2 digit, BCD signal representing the measured noise figure in dB.

NOI
GENER
+2

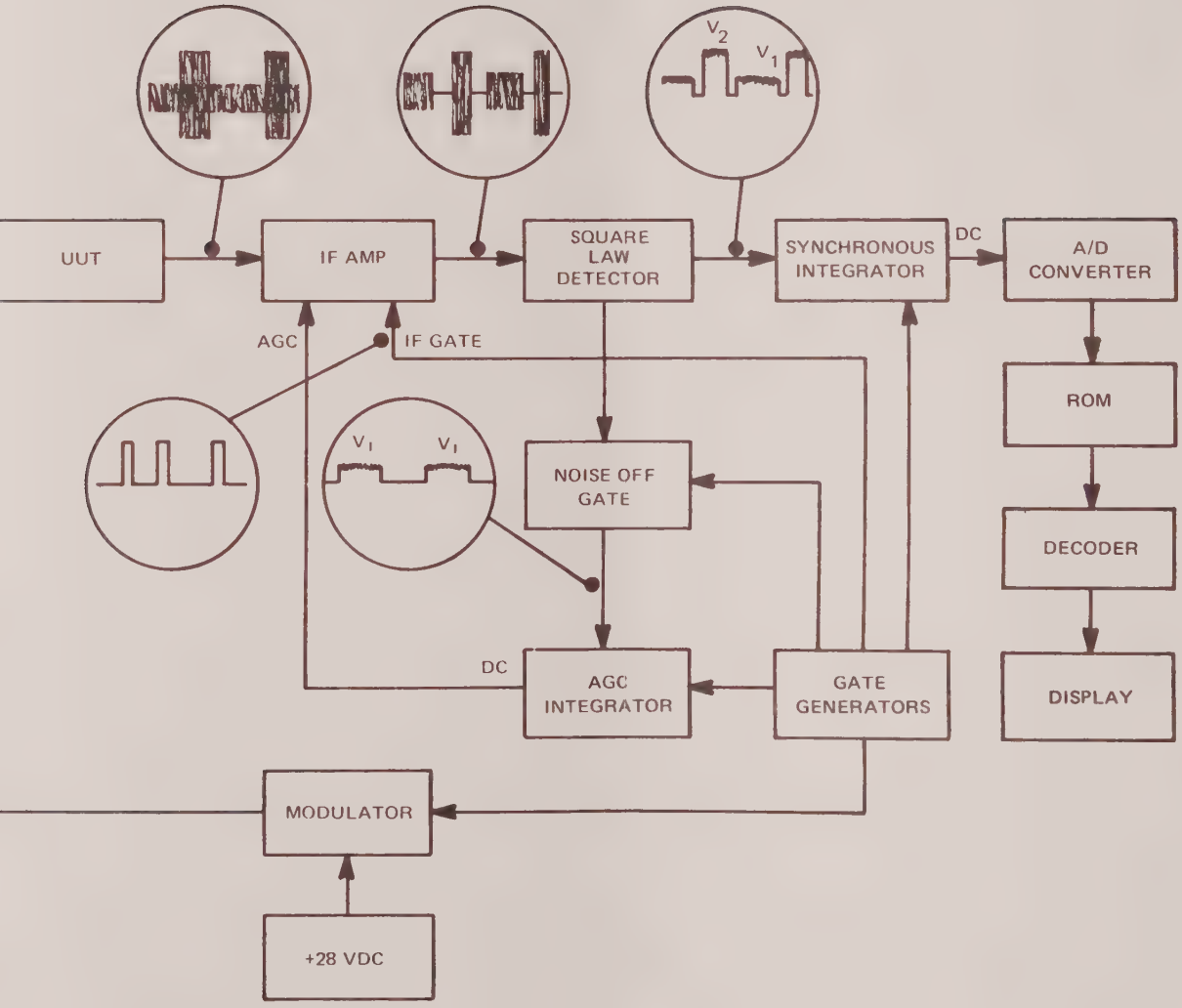


Figure 4-4. Functional Block Diagram

4-15. CIRCUIT DESCRIPTIONS

4-16. The following paragraphs describe the operation of the circuits within the System Noise Monitor. The order in which each description is presented generally follows the primary signal path rather than by complete sub-assembly description. Schematics will be found in Chapter V, Maintenance and Adjustments. The diagrams are printed on fold-out sheets so that they can be followed simultaneously with the circuit descriptions.

4-17. IF Amplifier. Signals applied to the IF input are transformer coupled via T101 to the first IF amplifier, Z101. C154 is adjusted for best input match, and the center frequency of the input stage is set by C102. T101 also provides a 2:1 voltage step-up.

4-18. The gain of the entire IF amplifier is controlled by application of the AGC signal to Z101. In the manual mode of operation, the AGC signal is replaced by a DC voltage set by R140. The AGC input will typically be between +5 volts at threshold and +7 volts at the high input level limit.

4-19. Additional IF gain is provided by Z102. The gain control input is driven by the IF gate to establish the zero noise reference. The IF gain of Z102 goes to zero when the gate signal goes positive. When MAN-AUTO switch S101 is set to the Manual mode, the narrow pulse pair is replaced by the output of the timing generator.

4-20. The output of Z102 is transformer coupled in a balanced configuration to the square-law detector. C114 tunes the output circuit to the SNM center frequency.

4-21. In a typical unit operating at the sensitivity limit, the overall IF gain will be about 35 dB. This will vary somewhat from unit to unit and at the various intermediate frequencies.

4-22. Square Law Detector. The detector, Z103, is a monolithic balanced modulator whose output contains a term proportional to the product of its two inputs. If the inputs are in parallel, then the output voltage is proportional to the square of the input voltage or the input power.

4-23. Since the input signal has three amplitudes — noise on, noise off, and zero reference — the detected output will be a three level signal with some low frequency noise on the noise on and noise off levels.

4-24. Variable Gain Amplifier. From equations 4-24 and 4-26 it can be seen that the calibration of the SNM for various noise generators with different ENR's can be maintained by changing the gain (proportionality constant) by the differences in dB. In the SNM, the calibration for a specific ENR is established by the gain of the two-stage video amplifier cascade, made up of Z105A and B. Each stage consists of an operational amplifier, operating in the inverting feedback mode; thus, the gains are determined by the feedback resistor values. These resistor networks are contained in 14 lead DIP's and are selected by the front panel thumbwheel switch.

4-25. Synchronous Integrator and Meter Amplifier. The three-level video signal is applied to the series-shunt switch combination made up of Z106C and D. Z106C clamps the output side of C140 to ground during the Noise-Off period. Z106D is a series switch which passes signals only during the Noise-on period. The clamping action of Z106C causes the amplitude of the video pulse at R122 to be equal to the difference between the Noise-On and Noise-Off signals. R122 and C131, in combination with Z107B form a non-inverting integrator.

4-26. R124 establishes the gain of Z107B and calibrates the analog section. R160 and R161 are used for a different version of the SNM and are not factors in the operation of the digital units. R150 is a balance adjustment on the operational amplifier and is used to set Z107B output to 0 ± 10 mV with no IF input signal. R125 establishes the voltage level applied to the Digital Board as well as the Recorder Output.

4-27. AGC Amplifier. The video output of Z104, the Video Driver (TP101) is also applied to the AGC Amplifier. This circuit is comprised of a series of gates, clamps, and amplifiers designed to provide a DC output proportional to the Noise-Off detector level. The high-gain requirements of the circuitry are fulfilled by AC amplification to reduce DC drift problems.

4-28. Z108A is a series switch that permits only the Zero Noise Reference and Noise Off detector level to be applied to the first amplifier Z104B. Z108B clamps the input of Z104B to ground except during the Noise Off period. Z108C, Z108D, R131 and C134 make up a synchronous integrator similar to that described in 4-25 except that the DC level developed is proportional only to the Noise Off detector level.

4-29. The DC signal is chopped (converted to AC) by Z110A and B, amplified by Z109A, and compared to a similarly chopped reference signal in differential amplifier Z111A. The reference signal is developed by zener diode CR101 and the voltage divider made up of R129 and R130. Z110C and Z110D convert the reference to AC in synchronism with the AGC signal. Z109B provides equivalent amplification.

4-30. The output of Z111A is synchronously integrated by Z112C, Z112D, R137 and C137. CR102 protects the analog gates from excessive reverse voltage when the input IF is below the AGC threshold. Z111B provides additional DC amplification. The output at TP104 will vary from about 5 volts at threshold to about 7 volts at the upper level limit. Z113A provides the Signal Monitor output. Z113B drives the front panel Signal Level lamp via Q101.

4-31. Timing Signal Generator. This circuit, consisting of three integrated circuit packages, provides the timing signals for the various analog gates and switches and the modulation gate for the noise source.

4-32. Z114A, Z114B, R146 and C138 make up a free-running oscillator which provides an asymetrical rectangular signal at about 550 Hz. This signal is inverted by Z114C and is used to drive the series switches of the AGC and AGC reference DC to AC converters and the final AGC synchronous integrator (Z110B, Z110C and Z112D).

4-33. The output of Z114C is again inverted by Z114D. The signal is the gating input for the noise source modulator and is also used to drive the shunt clamps in the AGC and AGC reference DC to AC converters and the final AGC synchronous integrator (Z110A, Z110D and Z112C).

4-34. Z115A and Z115B make up a one-shot multivibrator driven alternately by the differentiated outputs of Z114C and Z114D. Z115A is a three-input NOR gate; therefore, its output is low at all times except when all three inputs are simultaneously low. This is illustrated by Table 4-2.

TABLE 4-2. 3-INPUT NOR CIRCUIT TRUTH TABLE

INPUTS			OUTPUT
A	B	C	
0	0	0	1*
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

*1 = HIGH OR TRUE
0 = LOW OR FALSE
FOR CMOS LOGIC: 0 = 0 to +3.5 volts
1 = 8 to +12 volts
(+ 12 volts VDD)

4-35. In the quiescent condition, the output of inverter Z115B is LOW because its input is returned through R149 to +12 volts. Thus, all three inputs of NOR-gate Z115A are LOW (R147 and R148 returned to ground), and its output is HIGH. When the positive going edge of the signal at Z114C output occurs, the input of Z115A is momentarily driven HIGH, causing its output to go LOW. This drop in voltage appears at the input to Z115B and the inverter output goes HIGH. Feedback to Z115A input causes the action to be regenerative, resulting in the output of Z115B being driven rapidly to +12 volts where it remains until C141 is charged to a sufficiently positive voltage for Z115B to start conducting. The regenerative action then reverses, and the output of Z115B is rapidly driven to zero. The time constant is such that the resulting pulse is about 100 microseconds wide. The entire sequence repeats on the positive going edge of the output from Z114D.

4-36. The overall result, after two inversions through Z114E and Z114F, is a positive pulse at the start of each Noise On and Noise Off period. This signal is used to gate the second IF amplifier (Z102) off, establishing the zero noise reference.

4-37. The output of Z114D and the IF gate are also applied to NOR gate Z116A. This results in a positive pulse equal to the Noise-On period, less the zero noise reference time. This is used to control the series synchronous integrator switch (Z106D) (see paragraph 4-25), and is applied to NOR gate Z116C connected as a simple inverter. The resulting signal at TP107 is the series AGC gate.

4-38. NOR gate Z115C is driven by the output of Z114C (TP105) and the IF gate. Its output is a positive signal equal to the Noise-Off period less the zero noise reference time. It is used to drive the shunt clamp in the synchronous integrator (Z106C), and inverter Z116B. The output of the inverter (TP108) drives the shunt clamp in the AGC input stage (Z108B) and first integrator (Z108C).

4-39. POWER SUPPLY BOARD

4-40. The AILTECH 7360/7370 SNM require four different voltages: +12 VDC at 200 mA, -12 VDC at 150 mA, +5 volts at 400 mA, and +28 VDC at less than 20 mA. All voltages are derived from individual monolithic regulators and are protected by current-limiting circuits. See Figure 5-17 for a complete schematic diagram of the power supply.

4-41. +12 Volt Regulator. The +12 volt output from Z201 is set by resistors R204, R205, and R206. Resistor R205 adjusts the +12 volt supply used to set certain threshold levels on the IF Video Board. The short circuit current of the +12 volt supply is determined by resistor R201. Capacitor C203 is a compensation capacitor while capacitor C204 acts as a noise filter.

4-42. -12 Volt Regulator. The -12 volt supply is regulated by Z202. Resistor R207 and R208 determine the exact value of the regulated output, which may vary from -11.8 VDC to -12.2 VDC. The short circuit current for the -12 volt supply is determined by resistor R209. Capacitor C208 is the compensation capacitor, while capacitor C207 filters noise.

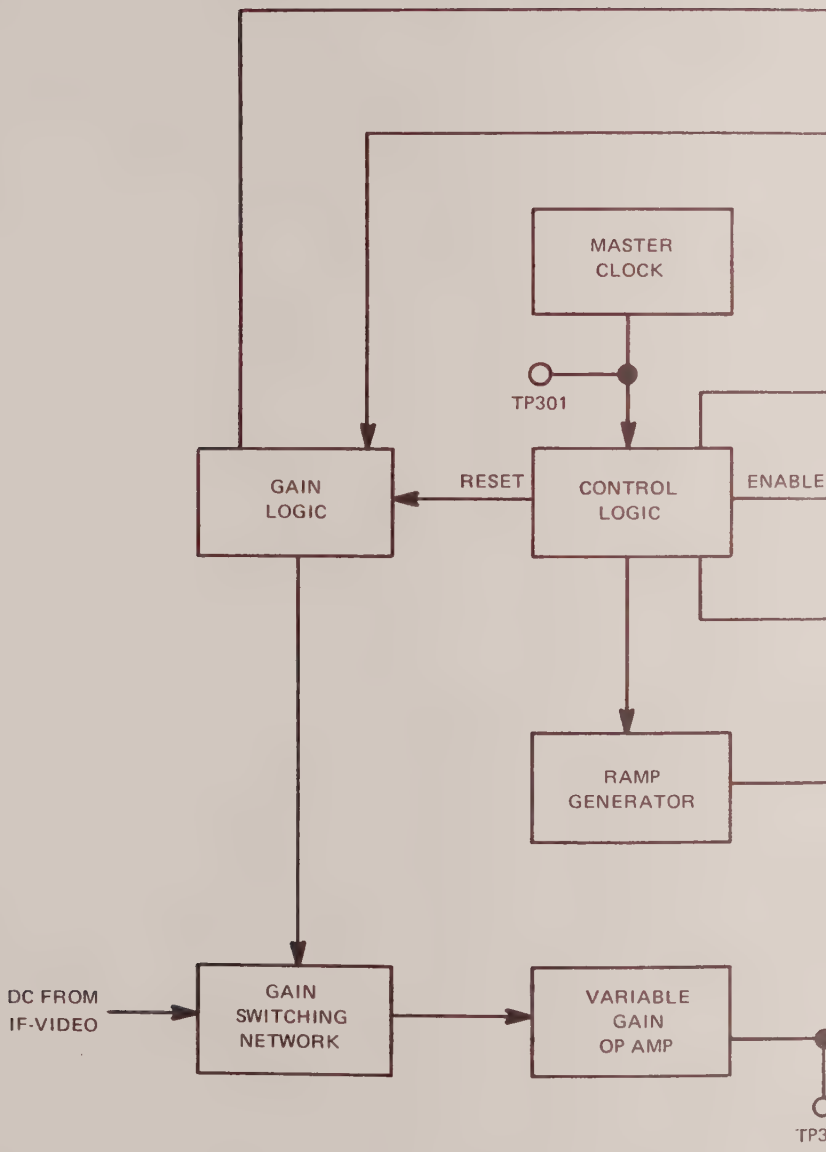
4-43. +28 Volt Noise Source Supply. The +28 VDC supply is regulated by Z203. A remote shutdown feature is designed into this supply to permit modulation by the 550 Hz clock on the IF Video Board. Transistor Q202 provides this capability. The 28-volt output can be precisely set by variable resistor R215. Resistor R212 provides short circuit protection. This supply is used exclusively to power the noise source.

4-44. +5 Volt Regulator. This voltage is used for the TTL circuits on the Digital P.C. Board. Unregulated +11 volts (nominal) is developed by full-wave bridge CR203 and filtered by C211. Regulation is provided by Z204, a three-terminal IC regulator with integral reference and compensation.

4-45. DIGITAL NOISE FIGURE CIRCUITS

4-46. Operational Description. The 7360/7370 digital circuitry is comprised of two P.C. Boards: the Digital Board and the Display Board. The Digital Board is made up of an ADC with automatic range capability, a ROM used as a look-up table, output latches and control logic. The Display Board consists of the display decoders and the LED seven segment displays. Figure 4-5 is a simplified block diagram of the digital circuitry.

4-47. The output of the IF-Video Board is a D.C. voltage that varies from 0 volts at 19.9 dB noise figure to about +7.5 volts at 0 dB noise figure. This signal is applied to an inverting operational amplifier whose gain can be switched to any one of six discrete values. The output of the operational amplifier, limited to prevent the voltage from becoming more negative than -4.7 volts, is applied to one side of a differential comparator. The opposite side of the comparator is driven by a negative going ramp that starts at 0 volts and terminates at about -5 volts. Whenever the ramp becomes more negative than the operational amplifier output, the comparator output switches from "High" to "Low".


MASTER
CLOCK
TP301
GAIN
LOGIC
RESET
CONTROL
LOGIC
ENABLE
RAMP
GENERATOR
DC FROM
IF-VIDEO
GAIN
SWITCHING
NETWORK
VARIABLE
GAIN
OP AMP

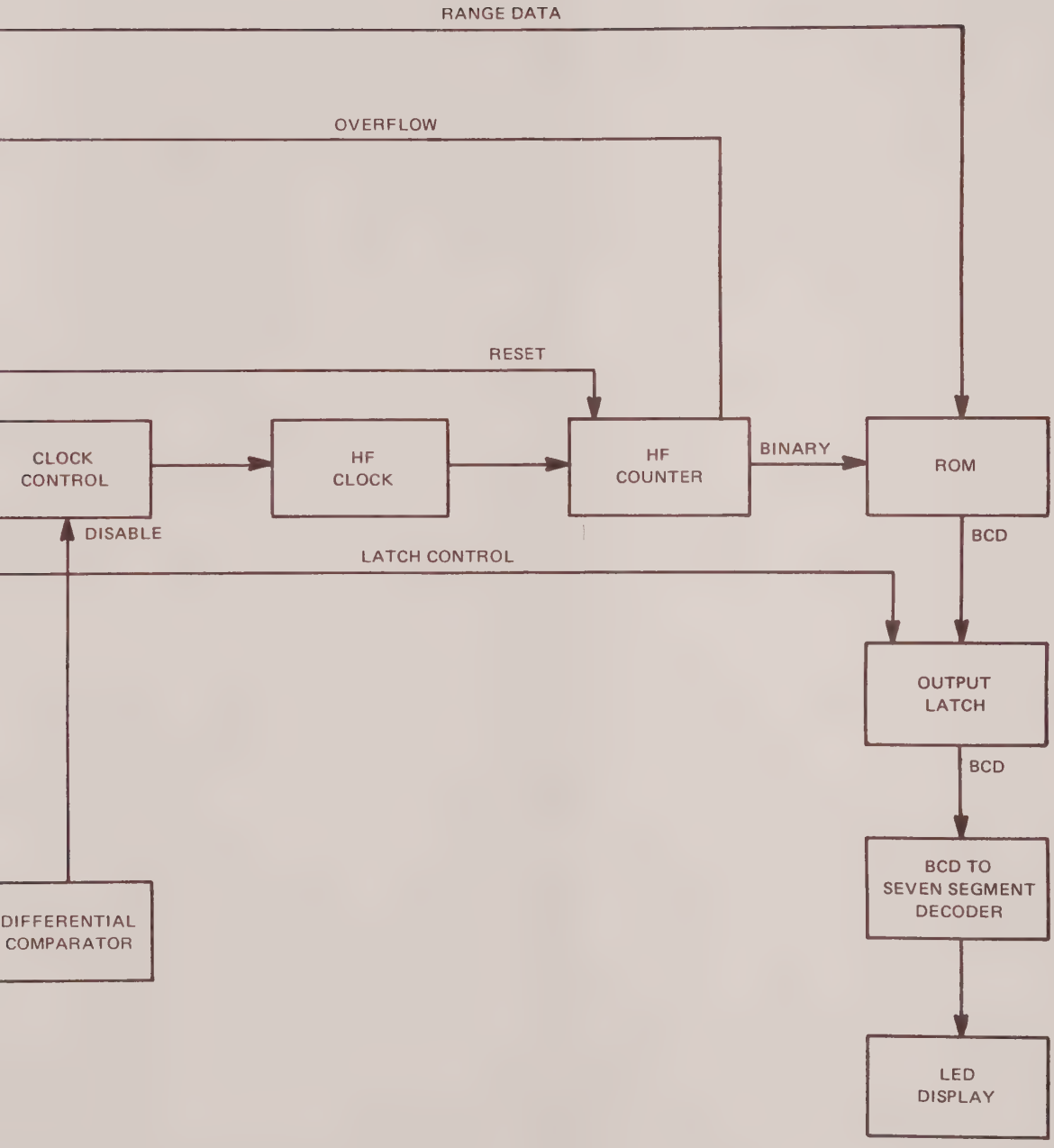


Figure 4-5. Digital Circuitry Simplified Block Diagram

4-48. The conversion cycle, which consists of eight A/D conversions, is sequenced by the control logic driven by the master clock. The actual A/D conversion is accomplished by a high-frequency (HF) clock gated on during the ramp period. The output of the HF clock drives a counter whose binary output represents the DC voltage input from the IF video board when the converter has selected the correct gain setting for the input amplifier. The binary data plus the range information is applied to the ROM which translates the data to noise figure in dB, in BCD parallel format. A latch holds the data for decoding and display. The BCD data is available at the rear panel.

4-49. At the start of the conversion cycle, the control logic:

a) Resets the gain of the input operational amplifier to its highest setting.

b) Resets the HF counter to zero.

c) Enables the ramp.

d) Starts the HF clock.

4-50. The HF counter counts the output of the gated clock and transfers the binary data to the ROM. If the measured noise figure is less than the lower limit of the range represented by the highest gain setting, the HF counter will produce an overflow signal before the ramp crosses through the amplifier output. The overflow signal causes the gain logic to switch the amplifier gain to the next lower value.

4-51. Near the end of the first 1/2 cycle of the master clock, the ramp becomes more negative than the clamped output of the operational amplifier, driving the comparator low, and turning off the HF clock. At the end of the first 1/2 cycle, the control logic resets the ramp to zero. Two 1/2 cycles later, the HF counter is reset to zero.

4-52. The sequence repeats, at the new operational amplifier gain setting, at the start of the third master clock cycle; thus, an A/D conversion is performed every other cycle of the clock. The process continues, with the operational amplifier gain reduced after each conversion, until a gain setting is reached such that the ramp becomes more negative than the amplifier output before the overflow signal is generated. The comparator disables the HF clock, and the count is held in the counter until reset just prior to the start of the next conversion.

4-53. Since an overflow signal was not generated, all subsequent conversions are performed at the same amplifier gain setting. All remaining conversions in the cycle should result in the same binary output from the HF counter.

4-54. The operational amplifier has six discrete gain settings; therefore, the ROM output is valid after six conversions no matter what the value of noise figure (assuming it is in the 0 to 19.9 dB range). Immediately following the sixth conversion, the control logic generates a latch pulse which transfers the ROM BCD data to the decoders. The data is latched and held until the sixth conversion of the next conversion cycle.

4-55. The general operation of the digital circuitry is further illustrated by Figure 4-6, Simplified Timing Diagram. All waveforms in this diagram are at TTL levels; however, Waveform D, the Ramp Output (solid line) and Variable Gain Operational Amplifier Output (dashed line), have been expanded vertically to show more detail. The waveforms shown are typical of those occurring when the measured noise figure is between 3.3 and 6.6 dB.

4-56. Waveform A is the Master Clock. Waveform B resets the gain logic so that the Variable Gain Operational Amplifier is at maximum gain at the start of the conversion cycle. Each conversion cycle requires 16 periods of the Master Clock. Waveform C is the Ramp Control Gate which occurs once every other period of the Master Clock. Waveform D shows both the Ramp and Operational Amplifier outputs and their time relation to other signals. These waveforms are shown for a noise figure between 3.3 and 6.6 dB for illustration purposes.

4-57. Waveform E enables the High Frequency (HF) Clock and Waveform F, the Comparator output disables the clock as indicated by the Clock Control Gate, Waveform G. Note that the timing of the clock disable pulse depends upon the amplitude of the operational amplifier output.

4-58. The HF Counter is reset just prior to the start of each conversion. The HF Clock rate is set so that an overflow signal occurs at about the midpoint of the ramp. This signal is the positive-going edge of Waveform I. Note that on the first four conversions the output of the operational amplifier is more negative than the ramp at the ramp midpoint and an overflow signal is generated. On the fifth and all subsequent conversions in the cycle, however, the Comparator output disables the HF Clock before the overflow signal can be generated. Since there are only six gain positions, the result must be valid after the sixth conversion, and is transferred to the display by the Output Latch (Waveform J).

4-59. DETAILED DIGITAL CIRCUIT DESCRIPTIONS

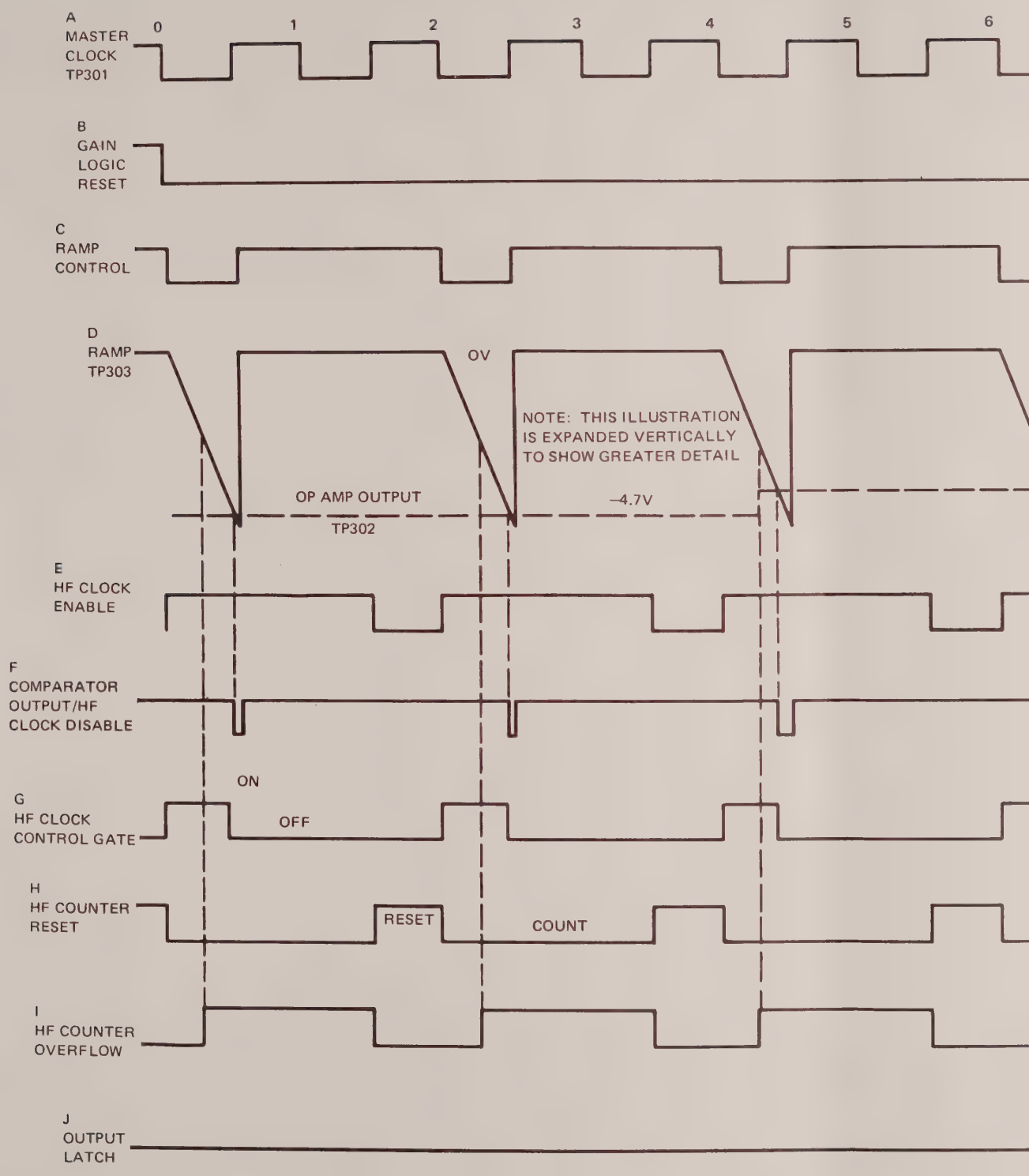
4-60. The schematic diagrams pertinent to these descriptions are Figure 5-19 and 5-20. These diagrams can be unfolded so they are visible and can be followed with the circuit descriptions.

4-61. Variable Gain Operational Amplifier. The analog D.C. information representing noise figure is applied to feedback amplifier Z301. The gain of Z301 is determined primarily by the ratio of the feedback resistor, R312, to the input resistor selected by the analog switches Z306 and Z307 (see Figure 5-5). R312 is connected to the common drain of the analog switches through J15. R313 and R314 are used only in a special multi-range option and are not functional in the standard Digital System Noise Monitors. Z302 is a non-inverting, unity-gain, voltage follower.

4-62. Only one of the analog switches is activated during any one conversion. Each gain setting corresponds to a specific noise figure range and, hence to a particular range of input voltages. See Table 4-3.

TABLE 4-3. VARIABLE GAIN OPERATIONAL AMPLIFIER CHARACTERISTICS

Noise Figure Range	Input Voltage Range (TP306)	Switch Closure	Op Amp Gain
0.0 to 3.3 dB	7.50 to 3.50 volts	Z307 — A	0.0 dB
3.3 to 6.6	3.50 to 1.64	— B	6.6
6.6 to 9.9	1.64 to 0.77	— C	13.2
10.0 to 13.3	0.75 to 0.35	Z306 — A	20.0
13.3 to 16.6	0.35 to 0.16	— B	26.6
16.6 to 19.9	0.16 to 0.08	— C	33.2


A
MASTER
CLOCK
TP301
0
1
2
3
4
5
6
B
GAIN
LOGIC
RESET
C
RAMP
CONTROL
D
RAMP
TP303
OV
NOTE: THIS ILLUSTRATION
IS EXPANDED VERTICALLY
TO SHOW GREATER DETAIL
OP AMP OUTPUT
TP302
–4.7V
E
HF CLOCK
ENABLE
F
COMPARATOR
OUTPUT/HF
CLOCK DISABLE
ON
G
HF CLOCK
CONTROL GATE
OFF
H
HF COUNTER
RESET
RESET
COUNT
I
HF COUNTER
OVERFLOW
J
OUTPUT
LATCH

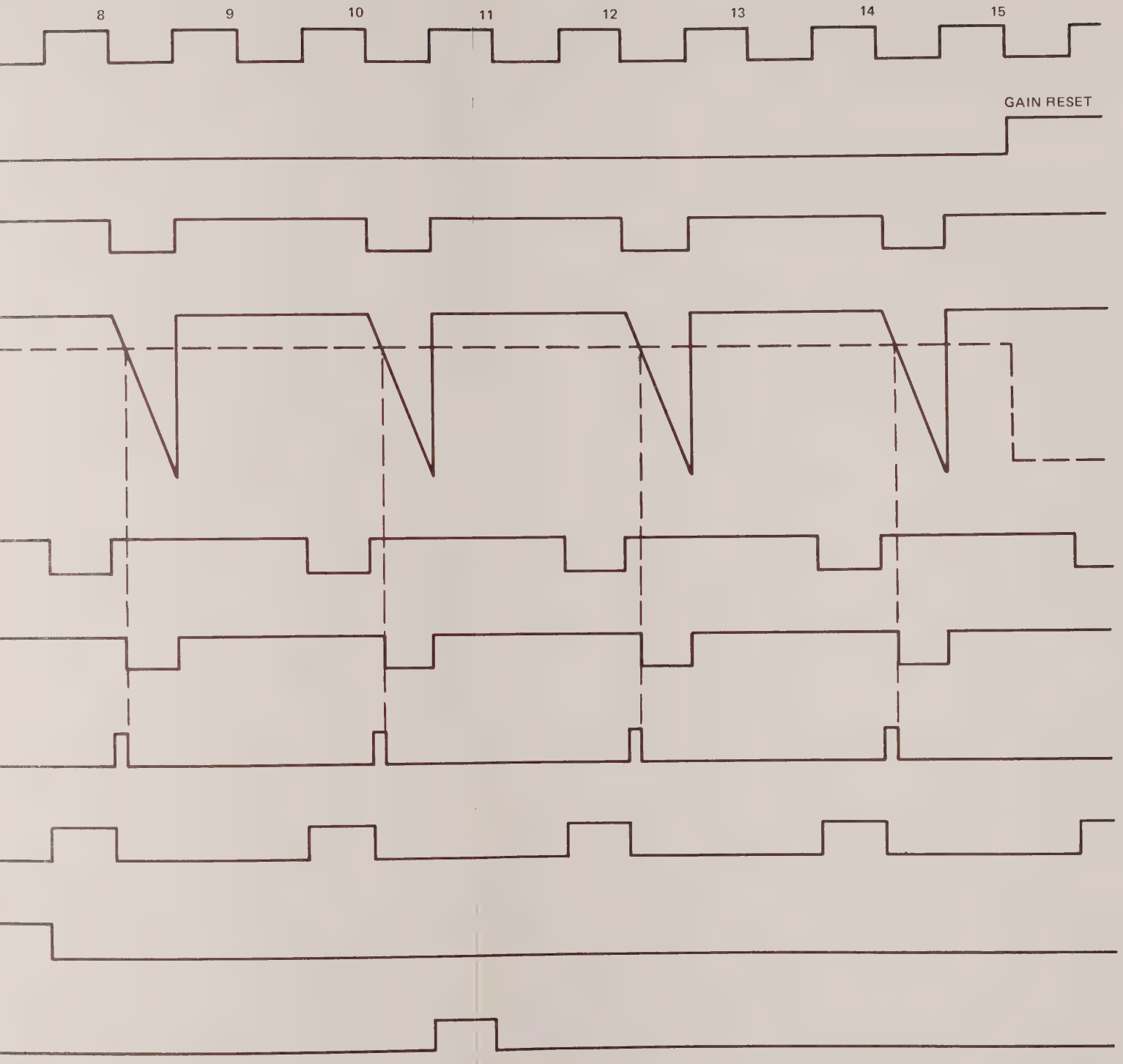


Figure 4-6. Digital Circuit Simplified Timing Diagram. Noise Figure Between 3.3 and 6.6 dB

4-63. The actual voltage at the output of voltage follower Z302 (TP302) is the product of the gain and the input voltage less 3.5 volts offset introduced by the voltage divider consisting of R316, R318 and R319, that is:

$$V_{OUT} = -(V_{in}G - 3.5) \qquad (4\text{-}27)$$

The output voltage cannot become more negative than -4.7 volts due to the zener diode CR301 at the output of Z301.

4-64. Ramp Generator. Z303 is connected as a standard, integrating operational amplifier. The ramp is gated on and off by analog switch Z305A. Application of a "Low" causes the switch to become a short circuit, discharging the integrating capacitor C306 and clamping the amplifier output near 0 volts set by R327. R329 in conjunction with C306 determines the ramp slope. It is set so that the ramp just reaches -5 volts during the ramp "on" control gate.

4-65. Comparator. Z304 is an operational amplifier with no feedback. Because of its high open loop gain its output is either "on" or "off". When the ramp applied to the non-inverting input becomes more negative than the analog D.C. applied to the inverting input, the output switches from a "High" to a "Low".

4-66. High Frequency Clock. The HF clock is made up of three NAND gates (see par. 5-44). The "A" and "B" sections of Z309 make up the oscillator. The frequency of oscillation, nominally about 360 kHz, is determined by C308, R320 and R321. The "C" section is used as an output driver, inverter, and a gate control. If any input of any NAND section is pulled "Low", the output will be interrupted.

4-67. All three sections have one input brought out for control purposes; however, the "B" section control input is hard-wired "High" through Z309. The "C" section input is controlled by Z333, an eight-input NAND gate, whose output is "low" only under the invalid condition when the input D.C. represents a noise figure less than 0.0 dB. This can occur if the front panel ENR switch is incorrectly set to an artificially low value. Z333 recognizes 0.0 dB and gates the output driver off, preventing this information from reaching the ROM and the display circuits. The "A" section is controlled by the "Q" output of flip-flop Z308B. When that output is "High", oscillations are sustained. When the output is "Low", the clock is turned off.

4-68. HF Clock Control. The comparator output is connected to the "Reset" input of flip-flop Z308B; thus, when Z304 output switches "Low", Z308B Q output switches "Low" causing the HF oscillator to cease oscillations. Oscillations are restarted when a positive going trigger is received at pin 3 of Z308B, the clock input. Since the data input is hard-wired to a high level through Z309, the Q output goes high, permitting the HF clock to run.

4-69. Ramp Control. The ramp generator, Z303, is controlled by the FET switch Z305A. A positive or "High" level at the FET gate causes the switch to become an open circuit, permitting the ramp generator to operate. A "Low" at the gate input short circuits the integrating capacitor C306, terminating the ramp.

4-70. The ramp switch control signal is derived from the Q output of flip-flop Z308A. The ramp is enabled by the same signal that starts the HF clock. The disabling signal is derived from the master control logic (Z312D).

4-71. Master Clock. The master clock is made up of three NAND sections (Z312A, B and C), and is similar to the HF clock except that the inputs of each NAND section are tied together. This permits the circuit to oscillate in a free-running mode at a nominal frequency of 1 kHz as determined by C309 and R315.

4-72. Control Logic. This circuit generates the various gates and signals that control the conversion cycle and is made up of binary counter Z313, NAND gates Z312D, Z316, Z317, and Z319, and inverters Z315 and Z318D. The counter is driven by the negative-going transitions of the master clock, and the binary output is combined with the clock output by the gates and inverters to ensure proper sequencing of the required signals during the conversion cycle.

4-73. Operation of the control logic circuit is illustrated in the detailed timing diagram, Figure 4-7. The waveforms shown are idealized for illustration; however, the sequence is what would be observed by an oscilloscope triggered by the negative transition at pin 10 of Z315 (Gain Logic Reset).

4-74. Gain Control Logic. The gain of the autoranging operational amplifier is controlled by the logic circuit made up of three-bit binary counter Z314, inverter Z318, and NAND gates Z320 and Z321. NAND gate Z322 is used to decode the gain setting into an address for the ROM.

4-75. Just prior to the start of a conversion cycle, the counter, Z314, is reset by a "High" on pins 1 and 2 derived from Z315 pin 10. With all counter outputs at zero, the decoder made up of the NAND gates Z320 and Z321 and inverters Z318A, B and C will pull the gate of analog switch Z306C low and hold all other gates of Z306 and Z307 high. This makes Z306C a short circuit and sets the gain of Z301 at maximum (R301 and R302 are the smallest of the input resistors). If the HF counter generates an overflow signal, this advances the counter, via Z318E, one step, and the decoder decreases the gain of Z301 by closing the next switch in line and open circuiting the previously closed switch. This operation is illustrated in more detail in Table 4-4, the Gain Control Logic Truth Table.

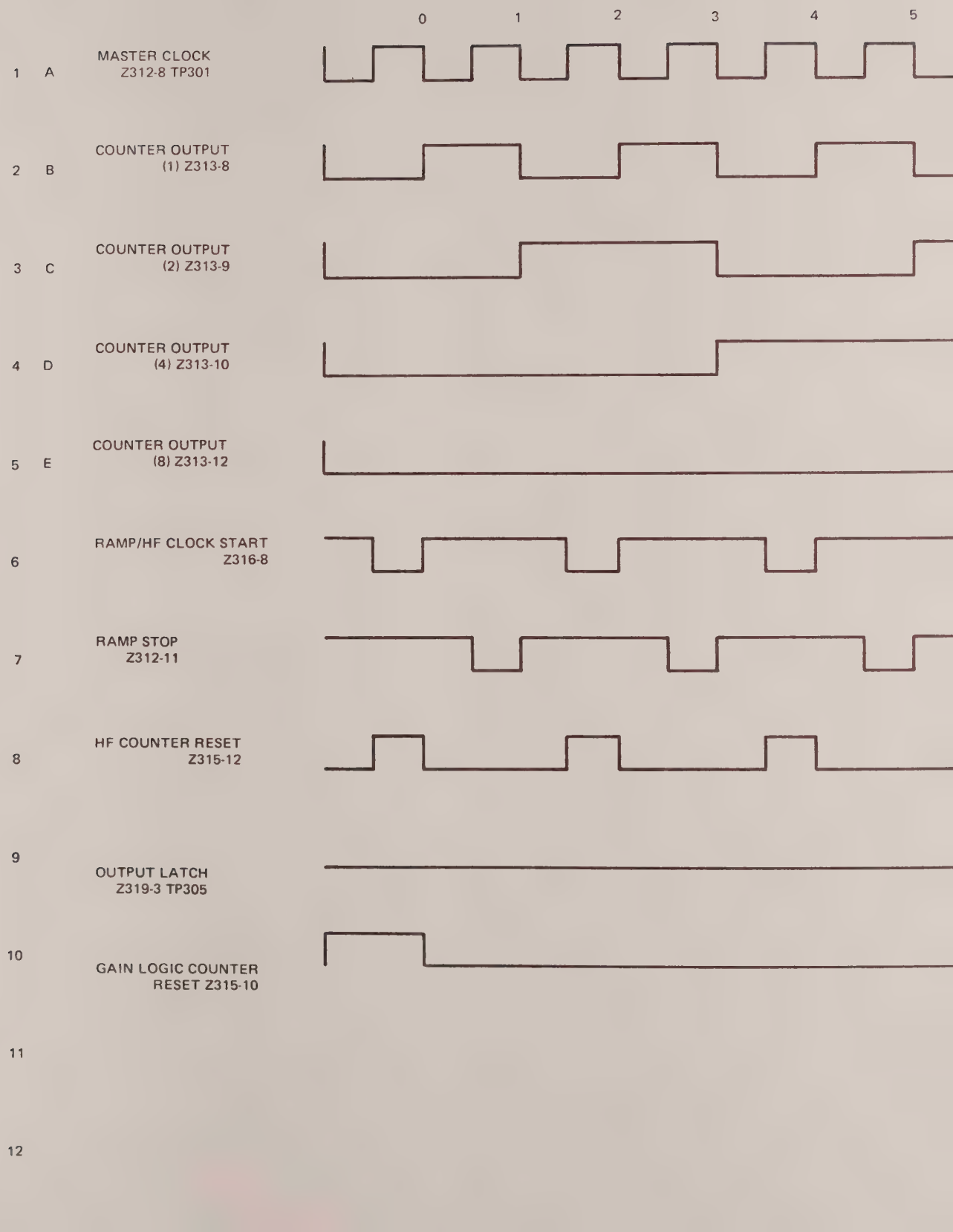
4-76. Data Output Circuit. The binary outputs of the HF counter and the two least significant outputs of Z322 (sections A and B) are applied to the ROM as an eight bit address. The ROM outputs are two, full, four-bit, BCD digits representing the units and tenths of dB's of noise figure.

4-77. These two digits are transferred to output latches Z326 and Z327 via NAND gates Z330 and Z329 respectively. The gates are hard-wired through Z328D as simple inverters. Since only one bit of information is required for the tens digit (maximum range of the instrument is up to 19.9 dB), that digit is derived directly from Z322C in the gain control logic circuit. It is outputted via one section of latch Z325.

4-78. Z325, Z326,and Z327 are four-bit binary latches which transfer data present at their inputs to their outputs upon receipt of a "High" latch pulse. This pulse is derived from Z319 pin 3 (TP305) and, as noted earlier, occurs just after the sixth conversion.

4-79. Z332A is used to suppress the first display digit whenever the measured noise figure is less than 10 dB. The three MSB complement outputs are essentially hard-wired "High" through Z331. If the noise figure is 10 dB or higher, Z322C output in the gain control logic circuit will be high and the LSB complement output of Z325 will be low. The output of Z332A, therefore, will be high, enabling the tens digit display decoder, Z401, on the Display Board.

4-80. If the noise figure is less than 10 dB, Z322C output will be low, the LSB complement output will be high, and Z332A output will be low. This will disable the tens digit display decoder and suppress the leading zero.


0
1
2
3
4
5
1 A
MASTER CLOCK
Z312-8 TP301
2 B
COUNTER OUTPUT
(1) Z313-8
3 C
COUNTER OUTPUT
(2) Z313-9
4 D
COUNTER OUTPUT
(4) Z313-10
5 E
COUNTER OUTPUT
(8) Z313-12
6
RAMP/HF CLOCK START
Z316-8
7
RAMP STOP
Z312-11
8
HF COUNTER RESET
Z315-12
9
OUTPUT LATCH
Z319-3 TP305
10
GAIN LOGIC COUNTER
RESET Z315-10
11
12

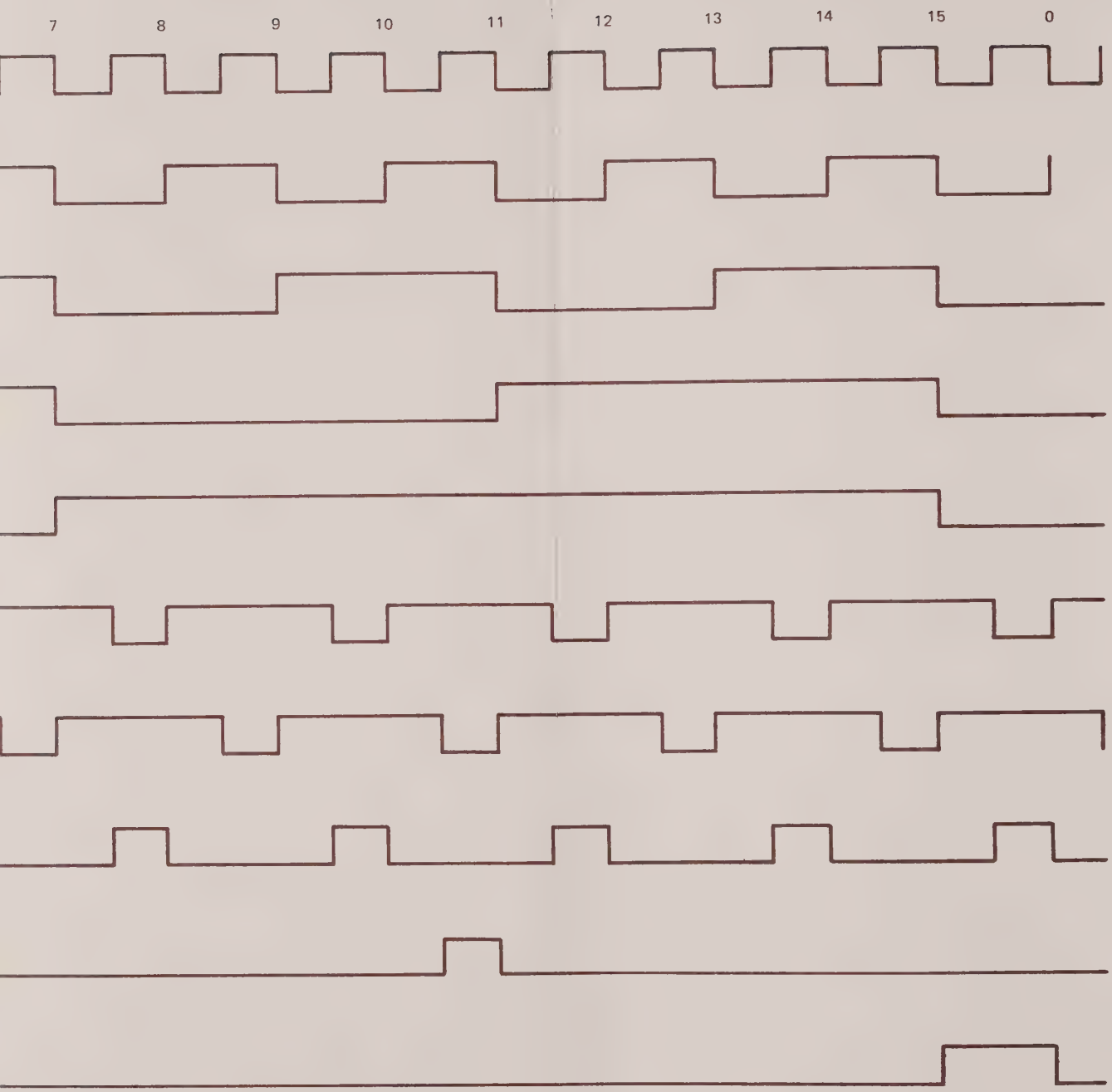


Figure 4-7. Control Logic Detailed Timing Diagram

TABLE 4-4. GAIN CONTROL LOGIC TRUTH TABLE

IC	Z314			Z318			Z320			Z321			Z322		
SECTION				A	B	C	B	A	C	B	A	C	B	A	C
PIN #	12	10	9	2	4	6	8	6	12	8	6	12	8	6	12
	0	0	0	1	1	1	1	1	1	1	1	0	0	0	1
	0	0	1	1	1	0	1	1	1	1	0	1	0	1	1
	0	1	0	1	0	1	1	1	1	0	1	1	1	0	1
	0	1	1	1	0	0	1	1	0	1	1	1	0	0	0
	1	0	0	0	1	1	1	0	1	1	1	1	0	1	0
	1	0	1	0	1	0	0	1	1	1	1	1	1	0	0

NOTE: 1 = "HI", +3 TO +5 VOLTS
0 = "LO", 0 TO +0.5 VOLTS

4-81. Option Circuitry. The AILTECH 7360 and 7370 SNM's are designed to permit simple installation of various options. For this reason:

a) Although shown on the schematic, Z324 is not installed; however, the socket is soldered into the board.

b) Z329 and Z330 are wired as simple inverters.

c) Z331 is wired for a constant "Low" output.

d) Z332B is not used.

4-82. Noise Figure Display Board. This small P.C. board, mounted on the front panel, contains three, seven segment LED displays and three BCD-to-seven-segment decoders. The BCD outputs of the latches are applied to the decoders which, in turn, drive the displays. The display inhibit connection of the "tens" digit decoder, Z401, is connected to pin 6 of Z332 on the digital board, the leading zero inhibit gate output. This connection is left open on the other two decoders.

4-83. The BCD noise figure data is also connected, directly in parallel with the decoders, to the rear panel auxiliary output connector, J1. Thus, this connector contains exactly the same data applied to the decoders. The output latch pulse is also available at J1.

CHAPTER V

MAINTENANCE AND ADJUSTMENTS

5-1. GENERAL

5-2. This Chapter contains Performance Verification, Adjustments, and Troubleshooting. Schematics, printed circuit board component locations, and wiring diagrams will be found at the end of the Troubleshooting section. Spares and replaceable parts are in Chapter VI.

5-3. PERFORMANCE VERIFICATION

5-4. The following procedures (recommended at 90 day intervals) are designed to insure the user that his AILTECH 7360 or 7370 is operating within specifications. Only those specifications critical to performance are checked. In some cases, more than one specification is verified by the same procedure. Where a specification is a function of adjustment, reference is made to the paragraph describing that adjustment.

5-5. Table 5-1 lists the test equipment required for performance verification.

TABLE 5-1. TEST EQUIPMENT REQUIRED FOR PERFORMANCE VERIFICATION

Description	Recommended Manufacturer and Model
Signal Generator, 10 to 100 MHz, calibrated output -90 to -30 dBm	Boonton 512
Digital Voltmeter, DC, 0 to 28 volts, 4½ digits.	Systron-Donner 7004A
Noise Source, frequency compatible with the input of the simulated UUT	AILTECH 7600 Series
Precision Variable Attenuator, continuously variable	AILTECH 3200 Series

5-6. Minimum Operating Level. This procedure checks the basic sensitivity of the SNM at its center frequency. Its primary purpose is to insure that the instrument is properly tuned. If the unit fails this check, refer to paragraph 5-54.

a. Connect a signal generator to the IF Input of the SNM. Set the generator frequency to the center frequency of the SNM. Set the generator output level to less than -80 dBm.

b. Increase the output level until the green Signal Level light on the front panel is illuminated. Increase the generator level an additional 5 dB.

c. Note that the generator level is less than -70 dBm.

5-7. Noise Generator Power. The purpose of this check is to insure that the voltage applied to the solid state noise generators is within specified limits. This voltage determines the excess noise ratio of the noise generator and the subsequent overall accuracy of the noise figure measurement. If the unit fails this check, refer to paragraph 5-54.

a. Connect a DVM to The Noise Source Output Connector.

b. Set AUTO-MAN switch S101 to MAN. Set Noise Generator ON-OFF switch S102 to OFF. Note that the DVM indicates less than 0.3 volts.

c. Set Noise Generator ON-OFF switch S102 to ON. Note that the DVM indicates 28.00 ±0.05 volts.

d. Disconnect the DVM. Connect an oscilloscope to the Noise Source output. Set AUTO-MAN switch S101 to AUTO, Noise Generator ON-OFF switch S102 to OFF. Note that the waveform is an asymmetrical rectangular waveshape with a positive level of +28 volts and a low level of zero.

5-8. Accuracy. This specification is defined as the maximum permissible deviation of the SNM indication (operating in the normal, automatic mode) from a manual Y-factor measurement on the same unit-under-test (UUT). The accuracy is checked by making a manual Y-factor measurement, calculating noise figure, and comparing the result to the automatic indication. In general, it is good practice to make several manual measurements and average the results. The manual measurement procedure was detailed in paragraph 3-45 and is repeated here for convenience.

a. Set up the equipment as shown in Figure 5-1. See paragraph 5-9 for UUT requirements.

b. Remove the top cover and locate MAN-AUTO switch S101, Noise Generator switch S102, and Manual Gain Control R140 on the IF-Video Board. (See Figure 3-5.)

c. Set MAN-AUTO switch S101 to MAN and Noise Generator switch S102 to OFF.

d. Set The Precision Attenuator to 0 dB, and adjust Manual GAIN control R140 for a convenient reference indication on the LED NOISE FIGURE readout (typically about 6 dB). If the signal level is too low to reach an indication less than 19.9 dB, the ENR thumbwheel switch may be set to a lower number. Note the indication.

e. Set Noise Generator switch S102 to ON. Note that the indication decreases.

f. Increase the setting of the Precision Attenuator until the indication returns to the reference noted in (d). Record the attenuation change. This is the Y-factor in dB. 10.77

g. Set Noise Generator ON-OFF switch S102 to OFF. Return the Precision Attenuator to its original setting. If the indication is not within ±0.1 dB of the original reference, repeat the measurement.

h. Calculate Noise Figure from Equation 3-3a, the AILTECH Noise Figure Slide Rule, or Figure 3-7. 5.1

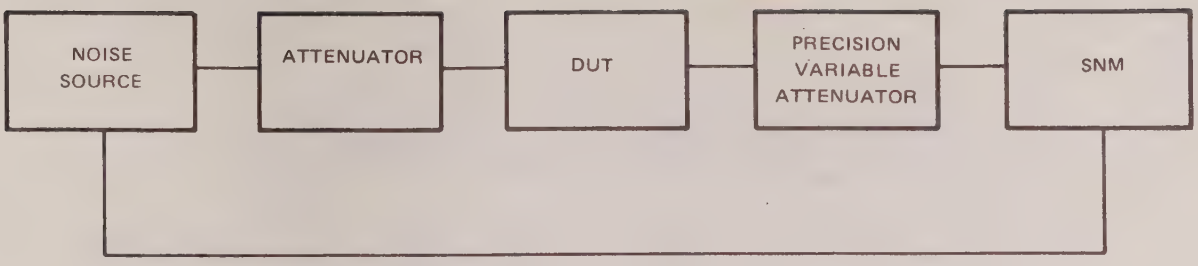


Figure 5-1. Set-up for Checking SNM Accuracy

i. If the noise figure is greater than 6 dB, recalculate the quantity based on an artificial ENR low enough to obtain that condition. Record the value of ENR used.

j. Bypass the Precision Attenuator. Set MAN-AUTO switch S101 to AUTO, Noise Generator ON-OFF switch S102 to OFF.

k. Set the ENR thumbwheel switch to the value recorded in Step (i). Note that the meter indication is within ±0.25 dB of the value calculated in Step (i). See paragraph 5-18 for adjustment.

l. Add sufficient attenuation between the noise source and the UUT and/or increase the ENR thumbwheel setting to obtain an indication between 6 and 12 dB (noise figure). Record the ENR setting.

m. Re-insert the Precision Attenuator, and repeat Steps (c) thru (g).

n. Calculate Noise Figure from Equation 3-3a, the AILTECH Noise Figure Slide Rule, or Figure 3-7. Use the ENR setting of Step (l) for the calculation.

o. Bypass the Precision Attenuator. Set MAN-AUTO switch S101 to AUTO, Noise Generator ON-OFF switch S102 to OFF.

p. Set the ENR thumbwheel switch to the value used to calculate the required noise parameter in step (n). Note that the indication is within ±0.5 dB of the value calculated in Step (n). See paragraph 5-18 for adjustment.

5-9. The simulated UUT used for this check must meet the same gain and noise figure conditions noted in paragraph 3-24; i.e. the "noise-on" signal must not be greater than 40 dB above the actual sensitivity as determined in paragraph 3-23, and the "noise-off" signal must not be less than the sensitivity. In addition, input and output frequencies must be compatible with the noise source and the SNM respectively.

5-10. CHECKS AND ADJUSTMENTS

5-11. Procedures for checking and adjusting the SNM are provided in paragraphs 5-13 thru 5-23. Adjustments on the IF-Video P.C. board in the 7360 and 7370 can be reached by pivoting the hinged Digital Board upwards after loosening the two captive thumbscrews. All other adjustments are available with just the top cover removed.

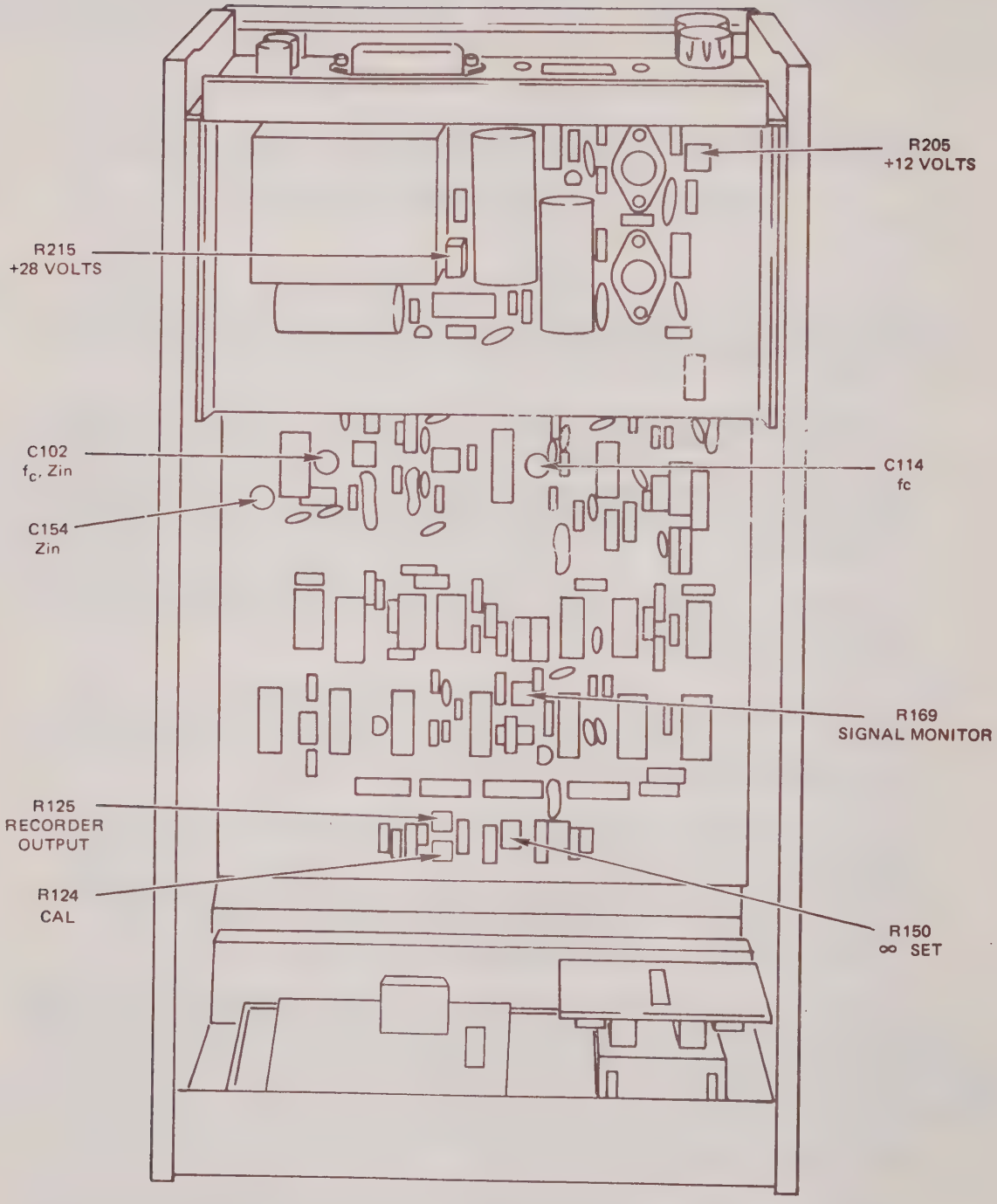


Figure 5-2 a) Adjustment Locations (Digital Board Removed)

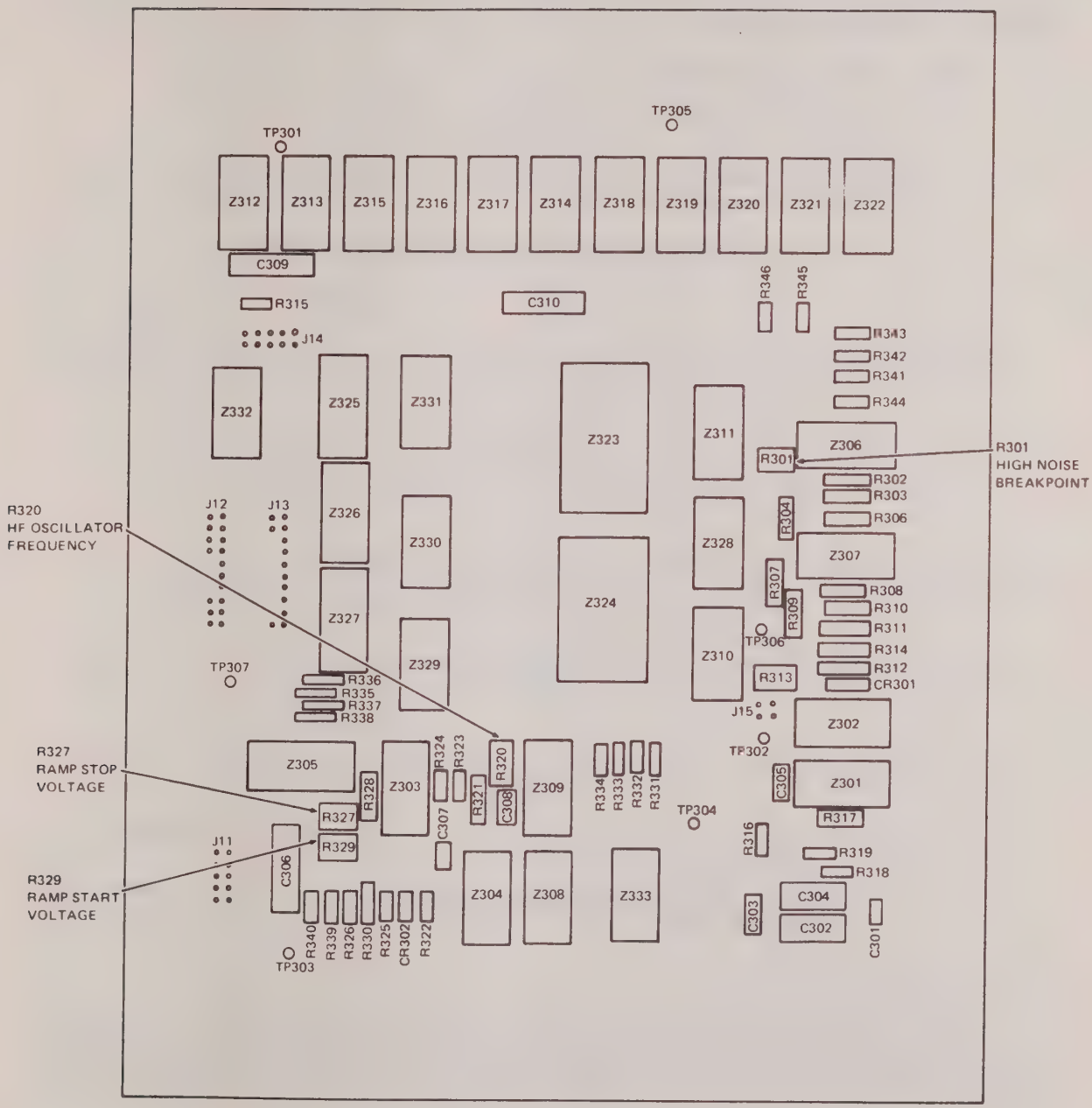


Figure 5-2 b) Digital Adjustment Locations

5-12. Components on the IF-Video P.C. Board have symbol numbers in the 100 to 199 range. Symbol numbers of power supply components are in the 200 to 299 range. Symbol numbers from 300 to 399 refer to the Digital Board while those in the 400 range are on the Display Board. Symbol numbers under 100 refer to components associated with the main chassis assembly. Test points on the printed circuit boards are marked only with the last digit; thus, TP 202 on the power supply board is marked simply "2".

5-13. POWER SUPPLY ADJUSTMENTS

a. All voltages are referenced to chassis ground.

b. Use a DVM and an oscilloscope with shielded leads to measure and adjust the power supplies in accordance with Table 5-2.

TABLE 5-2. POWER SUPPLY CHECKS AND ADJUSTMENTS

Test Point	Adjust	Voltage Vdc	Max. Ripple mV, p-p	Notes
201		+20 ±3	800	
202	R205	+12 ±0.05	5	
203		-20 ±3	400	
204		-12 ±1	5	
205		+40 ±6	200	
206	R215	+28 ±0.05	40	1
206		0 ±0.2	N/A	2
207		+11 ±1	800	
208		+5 ±0.25	10	

NOTES: 1. MAN-AUTO switch S101 set to MAN, Noise Generator ON-OFF switch S102 set to ON.

2. MAN-AUTO switch S101 set to MAN, Noise Generator ON-OFF switch S102 set to OFF.

5-14. IF ADJUSTMENTS

5-15. There are three interacting adjustments in the IF circuit C154, C102, and C114. C154 and C102 affect the input impedance and center frequency; C114 affects center frequency. If these adjustments are improperly set, the unit could appear low in sensitivity (minimum operating level too high).

5-16. Preliminary

a. Set MAN-AUTO switch S101 to MAN.

b. Set Noise Generator ON-OFF switch S102 to OFF.

c. Connect a signal generator set to the center frequency to the IF Input. Adjust the output level for about 10 dB NOISE FIGURE indication.

5-17. Procedure

a. Adjust C102, C114 and C154 for minimum NOISE FIGURE indication (C154 will have the least effect).

b. Connect the vector voltmeter to the IF input and adjust C102 and C154 for a reflection coefficient of less than 0.1.

c. Connect the signal generator to the input and readjust C114 for minimum NOISE FIGURE indication.

d. Check Minimum Operating Level as described in paragraph 5-6.

5-18. CALIBRATION ADJUSTMENTS

5-19. These adjustments insure the basic accuracy of the instrument. They should be varied only if the Performance Verification Check of paragraph 5-8 so indicates.

a. Connect a digital voltmeter (DVM) to TP103. Set MAN-AUTO switch S101 to AUTO, Noise Generator ON-OFF switch S102 to OFF, ENR thumbwheel switch to 10.0 dB. With no signal connected to the IF Input, adjust R150 until the DVM indicates less than ±10 mV.

b. Perform the calibration check described in paragraph 5-8 (steps a thru k). If necessary, adjust R124 to bring the AUTO indication within ±0.25 dB of the manual measurement result. If R124 has insufficient range, adjust R125.

c. Perform the high range calibration check described in paragraph 5-8 (steps l thru p). If the AUTO indication is not within ±0.5 dB of the manual measurement result, repeat steps a and b above.

d. If the specified accuracies cannot be met by means of the above adjustments, proceed to paragraph 5-20.

5-20. DIGITAL ADJUSTMENTS

5-21. The four adjustments on the digital board should not be disturbed unless it has been definitely established that the specified accuracies cannot be met by means of the calibration adjustments detailed in paragraph 5-19.

5-22. The digital board can be adjusted using an actual noise signal; however, because of the random nature of such signals it is difficult to reach the level of precision necessary to achieve the overall accuracy specification. For this reason it is recommended that a stable, variable, D.C. voltage be substituted for the output of the synchronous integrator operational amplifier, Z107B. The required voltages are in the range from 0 to +8 volts.

5-23. The recommended method of substitution is to remove Z107 from its socket, connect the positive lead of the substituted DC voltage source to TP103 and the negative lead to a convenient ground on the IF-Video Board.

5-24. Initial Settings

5-25. The following procedure, setting initial conditions, is usually necessary only in the event of a major malfunction requiring replacement of Z301, Z302, Z303, Z306, Z307 or Z309.

5-26. a. Connect an oscilloscope to TP304. Remove Z308 from its socket. Adjust R320 until the period of the rectangular waveshape is 2.75 microseconds. Note that the amplitude is 3 to 4 volts peak-to-peak. Replace Z308.

b. Connect an oscilloscope to TP303. The signal should be a negative going ramp. Adjust R329 so that the ramp starts at 0 volts.

c. Adjust R327 so that the ramp terminates at -5 volts.

5-27. Calibration Settings

5-28. Ramp Slope

a. Connect a DVM between TP306 and the analog ground on the digital board.

b. Adjust the substituted voltage source at TP103 until the DVM reads +3.562 volts. If an actual noise signal is being used, set S101 to MANUAL and adjust R140 for the voltage noted.

c. Adjust R329 until the LED NOISE FIGURE display flickers between 3.1 and 3.2 dB.

5-29. H.F. Clock Frequency

a. Adjust either the noise input or the substituted voltage until the DVM connected to TP306 reads +7.375 volts.

b. Adjust R320 until the LED NOISE FIGURE display flickers between 0.0 and 0.1 dB.

c. Recheck the Ramp Slope per paragraph 5-28. If it requires readjustment, repeat both 5-28 and 5-29 until no further adjustment is required.

5-30. High Noise Breakpoint

a. Adjust either the input level or the substitute voltage until the DVM at TP306 reads +0.078 volts.

b. Adjust R301 until the display flickers between 19.7 and 19.8 dB.

c. Repeat the Performance Verification Check of paragraph 5-8 and the Calibration Adjustments of paragraph 5-18 if necessary.

5-31. AUXILIARY OUTPUT ADJUSTMENTS

5-32. These adjustments are not critical to instrument performance, and need be set only if the user requires these auxiliary outputs.

5-33. Signal Monitor

a. With MAN-AUTO switch S101 in AUTO, apply an input signal at the center frequency to the IF Input. Increase the level until the front panel SIGNAL LEVEL light just comes on.

b. Connect a DVM between pin 4 of J1 (rear panel) and ground (pin 5 of J1).

c. Adjust R169 until the meter indicates 0.0 ±0.5 volts.

d. Increase the signal generator output level by 50 dB. Note that the DVM indication increases to about +5 volts.

5-34. Recorder Output. Because this output is used to drive the Digital Board, the adjustment, R125, should not be disturbed after the calibration adjustments (par. 5-18) have been performed. If it is desired to set the recorder output for a specific level, it will be necessary to recalibrate the instrument as detailed above.

5-35. TROUBLESHOOTING

5-36. Performance verification and the checks and adjustments of the proceeding paragraphs are valuable aids to locating malfunctions within the SNM. In addition, the troubleshooting flowcharts, Figures 5-10 thru 5-15, are designed to isolate problems to a particular circuit area.

5-37. GENERAL INFORMATION

5-38. Tools

a. A special tool is required for servicing the connectors in the SNM. This is available from AMP Inc. by ordering Connector Tool, P/N 91084-1. Instructions for use are provided with the tool.

b. Integrated circuits should be removed from their sockets using an extraction tool to minimize pin damage. A typical tool is the Augat Model T114-1.

c. Measurements taken directly from IC pins are facilitated by a spring clip designed for that purpose. Typical types are the Pomona DIP-CLIP Models 3914 and 3916.

5-39. Transistors. Plastic encapsulated transistors are used exclusively throughout the SNM. Figure 5-3 illustrates the physical configuration used.

5-40. Integrated Circuits. Both linear and digital IC's are used in the SNM. Figure 5-4 illustrates the physical configurations used, and Figure 5-5 provides functional descriptions.

5-41. Logic Family

5-42. All digital integrated circuits on the IF-Video P.C. Board are COS/MOS devices. Positive logic is used throughout, so a "True" condition is high, and a "False" condition is low. High and low voltage values are, in practice:

True (High or logical "1") = +8 to +12 volts
False (Low or logical "0") = 0 to +3.5 volts

These values are for a nominal supply of +12 volts.

5-43. The logic family used on the Digital P.C. Board is TTL. Positive logic is used; therefore,

True (1) = +2.5 to +5.0 volts
False (0) = 0 to +0.8 volts

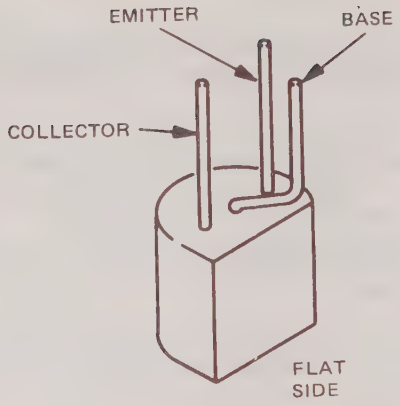


Figure 5-3. Plastic-Case Transistors

5-44. Logic Gates. Two general types of logic gates are used in the digital SNM's. These are the NOR (inverted OR) and NAND (Inverted AND) gates. The NOR gate is characterized by the fact that its output is always LOW except when all its inputs are simultaneously LOW. The NAND gate output is always HIGH except when all its inputs are simultaneously HIGH. This is illustrated for 3-input gates in Figure 5-6. The basic principles hold for gates with more or less inputs.

5-45. Analog Switches. Two types of analog switch or gate, which pass or block analog signals depending upon the condition of a control signal, are used in the SNM. On the IF-Video board these gates are generally used in series-shunt pairs to form DC to AC converters (choppers) or the inverse function, AC to DC converters (synchronous integrators). On the Digital board the gates are used as true switches in the autoranging A/D converter.

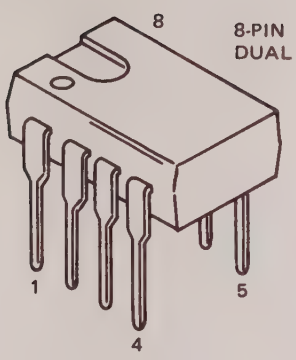
5-46. Although the gates are complex integrated circuits, they are, for simplicity, shown as FET's on the schematics. Operation of the COS/MOS N-channel switches used on the IF-Video board is illustrated by Figure 5-7. Operation of the P-channel devices (IH5012C and IH5014C) used on the Digital board is reversed; that is, the switch is a short circuit upon application of a LOW to the control input.

5-47. Flip-Flops. D-type, positive-edge-triggered flip-flops are used on the Digital board. Information at the input (D) is transferred to the output (Q) whenever a positive-going transition occurs at the clock input. The complementary output ($\overline{Q}$) is also available. Each circuit has independent Clear and Preset inputs which operate as follows: a LOW input to Clear sets the output LOW; a LOW input to Preset sets the output HIGH. These inputs operate independently of the Clock.

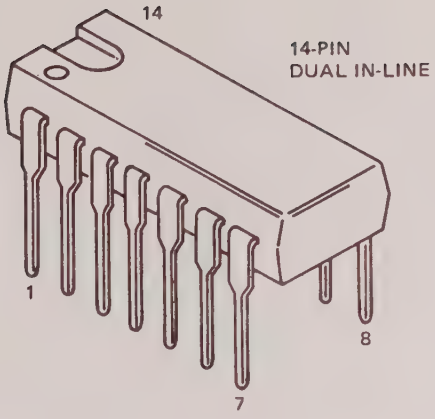
5-48. Operational Amplifiers. Operational amplifiers are used to implement many functions, such as summers, buffers, differential and offset amplifier. Figure 5-8 illustrates some typical circuits.

5-49. Printed Circuit Boards. The printed circuit boards (PCB's) used in the AILTECH 7300 SNM's are double-sided with plated-through holes; that is, there are conductor patterns on both sides of the boards, and connections from top to bottom are via metallic plating of through holes.

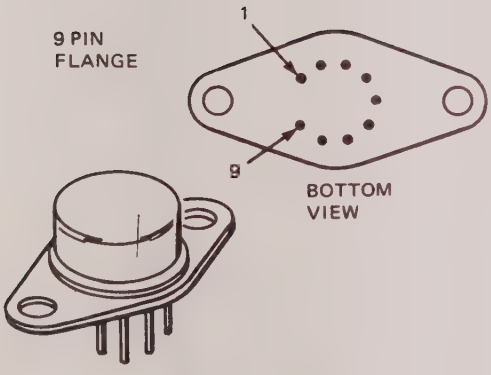
5-50. The PCB's are susceptible to damage from excess soldering heat. Use a soldering iron of less than 60 watts rating when working on the 7300 PCB's, and use a suction device to remove excess solder from component mounting holes. If possible, when replacing a component, clip the leads of the device to be replaced close to its body; thus, the old leads can be used as wrap-around



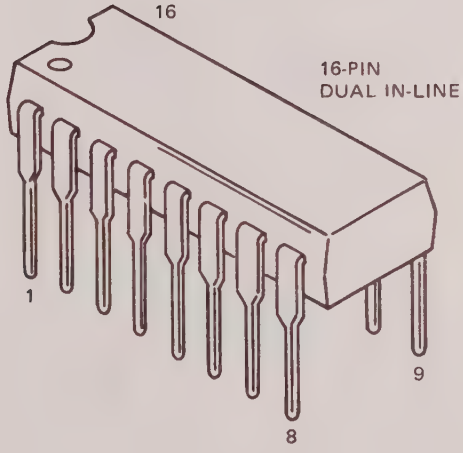
CASE A



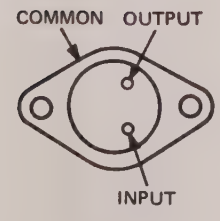
CASE B



CASE C



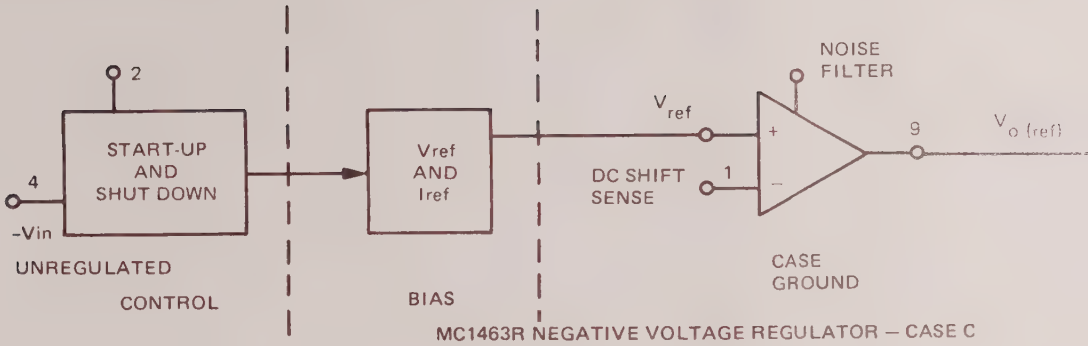
CASE D



CASE E

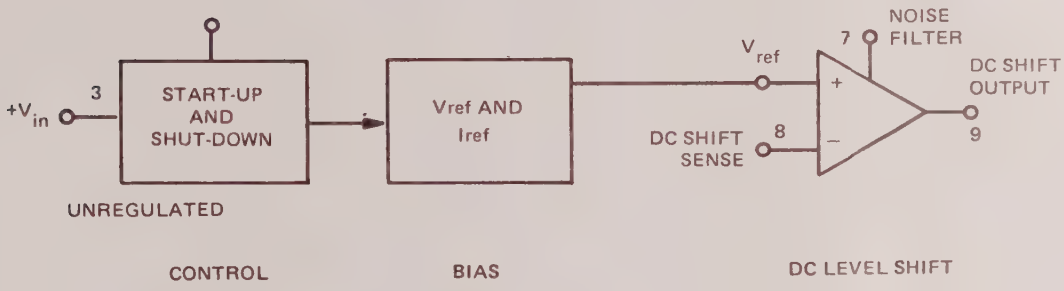
Figure 5-4. Integrated Circuit Case Styles

MC1463 BLOCK DIAGRAM

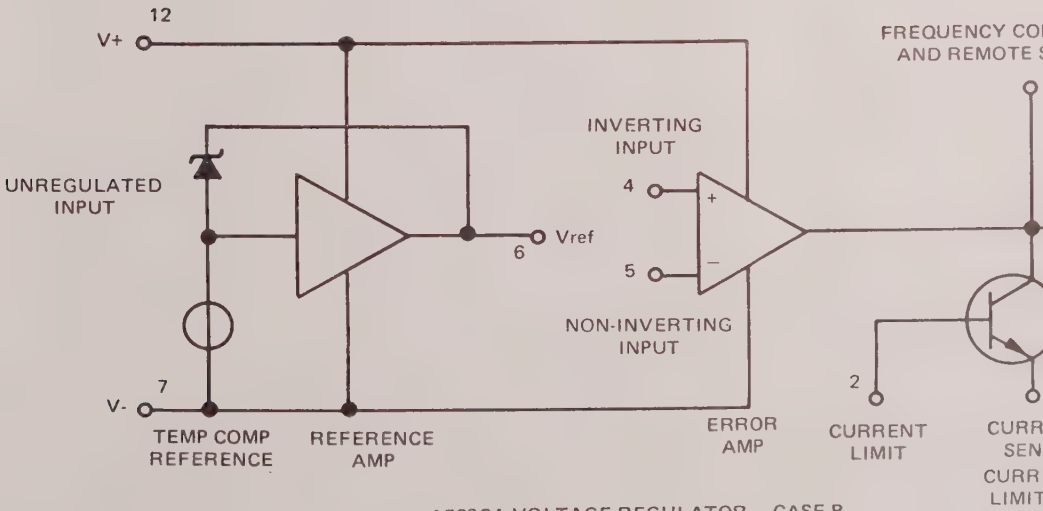


MC1463R NEGATIVE VOLTAGE REGULATOR – CASE C

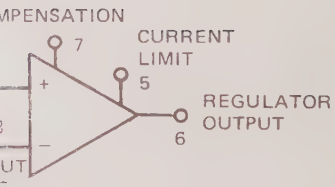
MC1469 BLOCK DIAGRAM



MC1469R POSITIVE VOLTAGE REGULATOR – CASE C

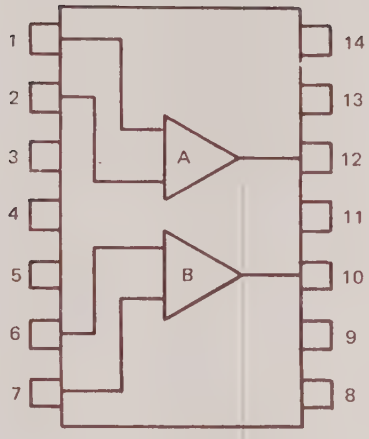


μA723CA VOLTAGE REGULATOR – CASE B



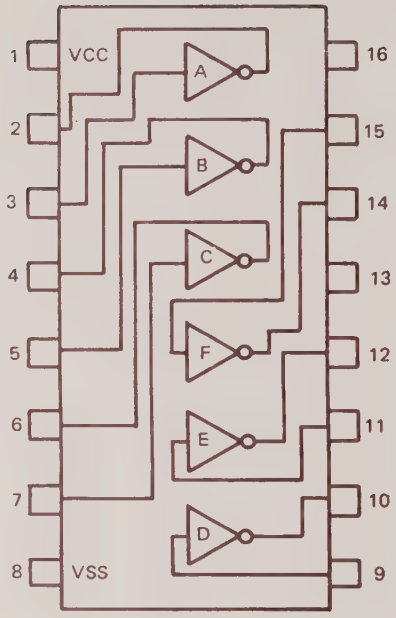
UNITY-GAIN REGULATOR

ERROR AMP AND
UNITY GAIN
REGULATOR



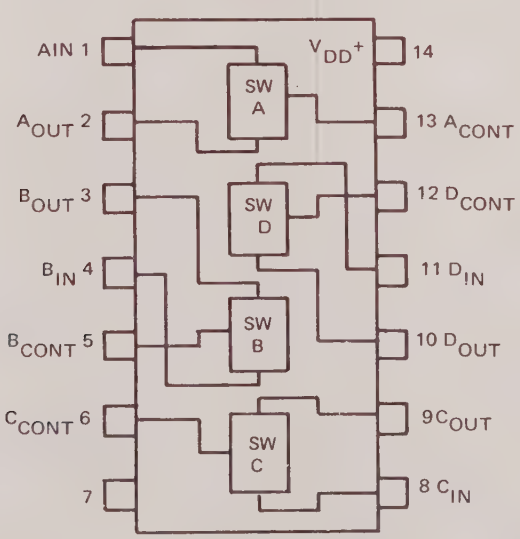
1. INV INPUT A
2. NON-INV INPUT A
3. OFFSET NULL A
4. V
5. OFFSET NULL B
6. NON-INV INPUT B
7. INV INPUT B
8. OFFSET NULL B
9. V + B
10. OUTPUT B
11. NO CONNECT
12. OUTPUT A
13. V + A
14. OFFSET NULL A

μA747CA DUAL OP AMP
CASE B



CD4000AE HEX INVERTER
CASE D

CD4016AE QUAD BILATERAL
SWITCH
CASE B



CD4000AE DUAL 3-INPUT
NOR GATE PLUS INVERTER
CASE B

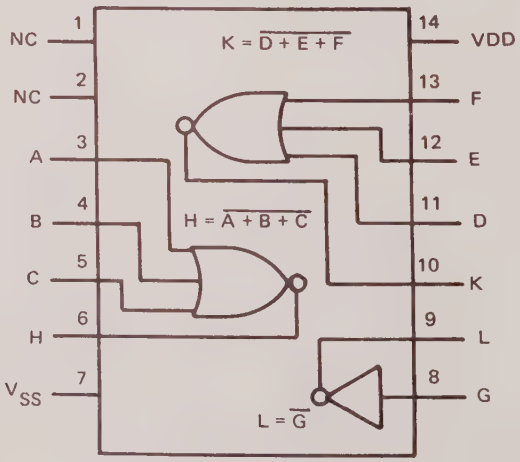
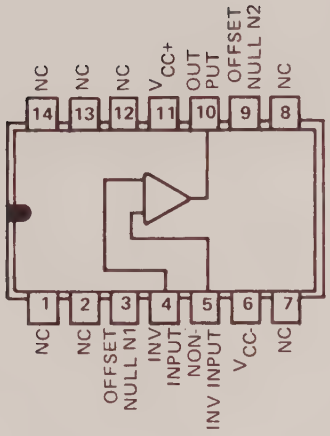
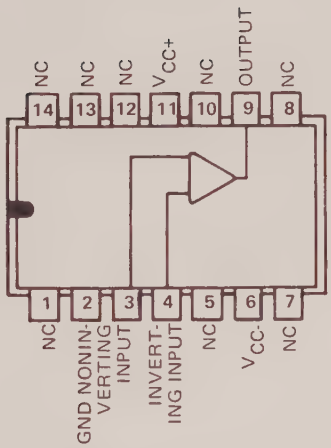


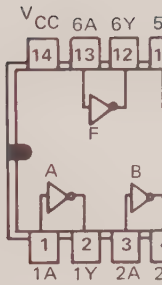
Figure 5-5. Integrated Circuits Functional Illustrations (Part 1)



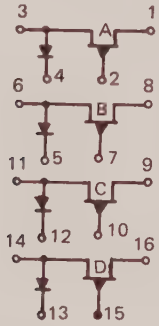
SN72741 OPERATIONAL
AMPLIFIER – CASE B



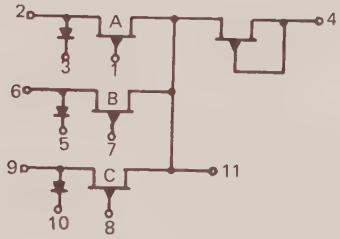
SN72710 OPERATIONAL
AMPLIFIER – CASE B



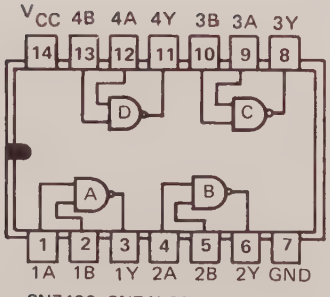
SN74L04 HEX
INVERTERS –



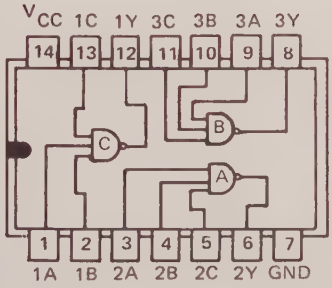
IH5012C
QUADRUPLE ANALOG
SWITCHES – CASE D



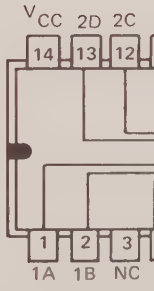
IH5014C TRIPLE
ANALOG SWITCHES,
COMMON DRAIN – CASE B



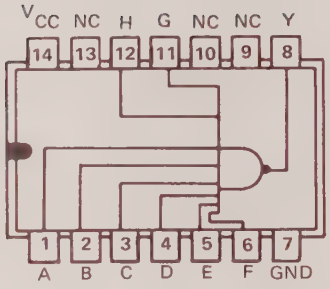
SN7400, SN74L00, AND
SN74L03 (OPEN COLLECTOR)
QUADRUPLE 2-INPUT
NAND GATES – CASE B



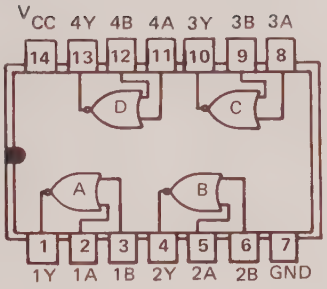
SN74L10 TRIPLE
3-INPUT NAND GATES
CASE B



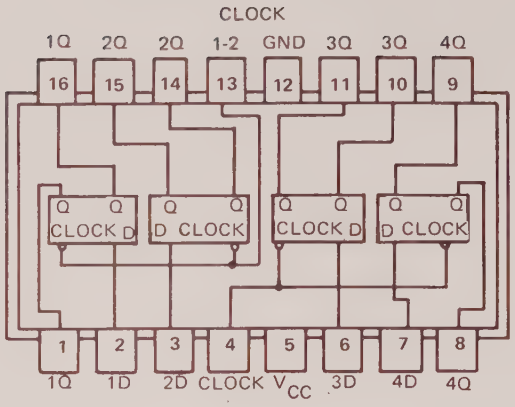
SN74L20 DUA
4-INPUT NAN
CASE B



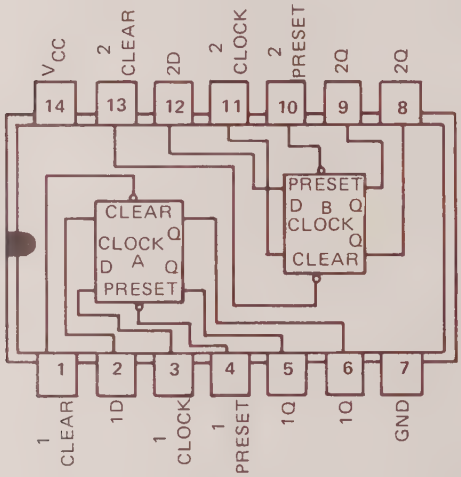
SN74L30 8-INPUT
NAND GATE – CASE B



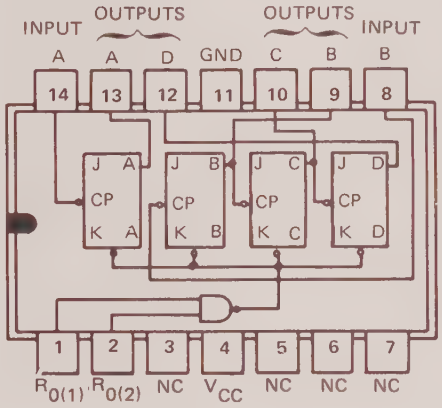
SN74L02 QUADRUPLE
2-INPUT NOR GATES
CASE B



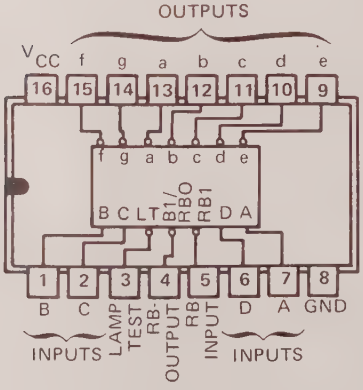
SN74100 4–BIT
BISTABLE LATCH
CASE – D



SN74L74 DUAL D-TYPE
POSITIVE-EDGE-TRIGGERED
FLIP-FLOPS CASE B

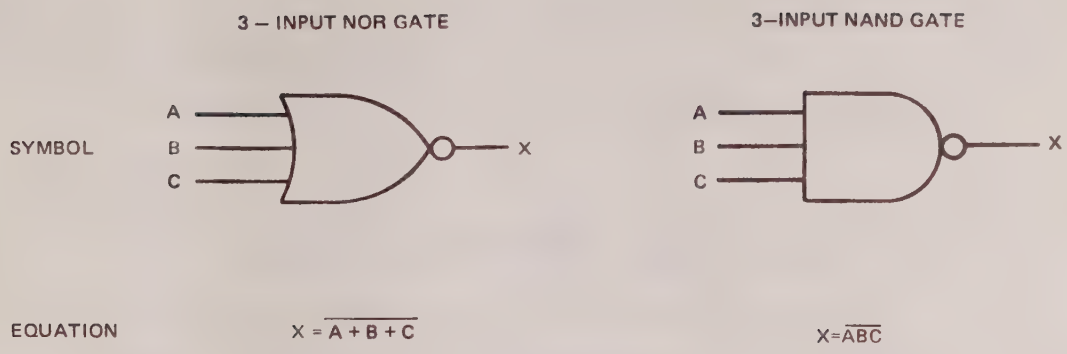


SN74L93 4-BIT BINARY
COUNTER – CASE B


OUTPUTS
VCC f g a b c d e
16 15 14 13 12 11 10 9
f g a b c d e
B C LT BI/RBO RB1 D A
1 2 3 4 5 6 7 8
B C LAMP TEST RB- OUTPUT RB INPUT D A GND
INPUTS INPUTS

SN74L47 BCD TO SEVEN
SEGMENT DECODER/DRIVER
CASE D

Figure 5-5. Integrated Circuits Functional Illustrations (Part 2)



TRUTH TABLE

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 5-6. 3-Input Logic Gate Operation

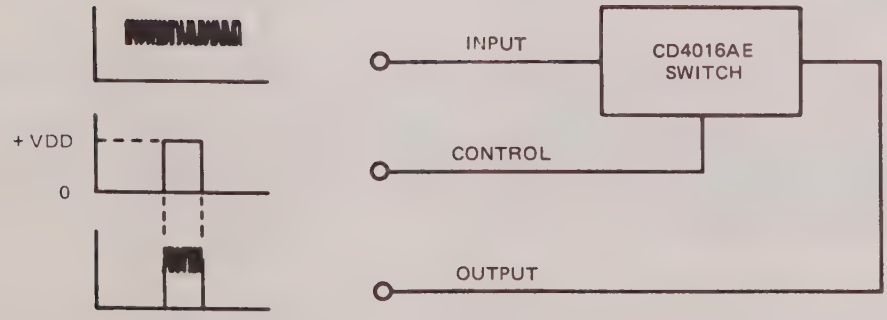


Figure 5-7. Operation of the COS/MOS Bilateral Switch

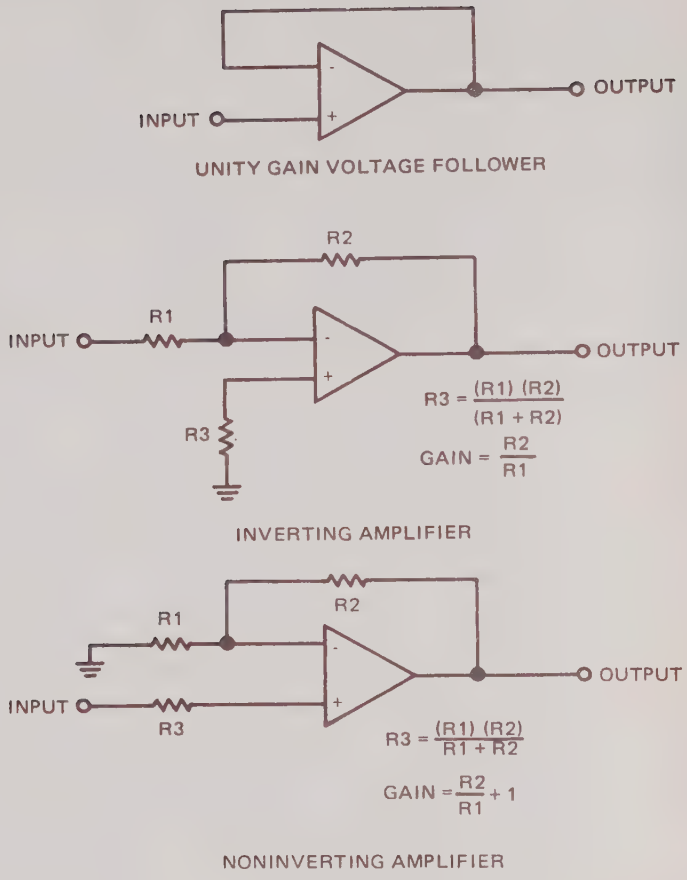


Figure 5-8. Typical Applications of Operational Amplifiers

terminals for soldering the new component in place. When soldering on the PCB's use a solder with a non-corrosive flux core, and clean the excess flux off the board after all soldering is complete. Damaged sections of the printed wiring can be repaired by soldering a length of bare, tinned copper wire across the damaged area.

5-51. Printed Circuit Board Connectors. Connections to the printed circuit boards are made via AMP type 87133-X. Connector tool, AMP P/N 91084-1 is required to service these connectors. Pin number layouts, as they appear on the boards are shown on the overall wiring diagram. In general, the pins are numbered consecutively with the numbers increasing in the same direction in each row (as contrasted to the continuous system used with IC's). This is illustrated by Figure 5-9 which is the layout of a 10 pin connector.

Figure 5-9. Pin Numbering Layout of a Typical AMP 87133 Connector
(View Looking Down on the Mating Pins)

5-52. Front Panel Lamps. DL-2, the Signal Level lamp is an incandescent lamp. In the event of a failure, the replacement procedure is as follows:

a. Strip the heat-shrink tubing from the connections on the rear of the lamp.

b. Unsolder the connections.

c. Using a pair of long-nose pliers, squeeze the three projections on the retainer clip together. Maintain pressure and slide the clip back off the lamp.

d. Remove the lamp from the front.

e. Reverse the removal procedure to mount the new lamp. Use insulated tubing over the solder connections.

5-53. ENR Thumbwheel Switch. This switch is held in place by spring loaded clips at the top and bottom and is removed from the front of the panel. To replace the switch simply remove the entire ENR Gain board by disconnecting the board edge connectors on the switch, depress the clips, and free the switch by rocking it back and forth in the vertical plane. The new switch may then be simply snapped into place.

5-54. TROUBLESHOOTING PROCEDURES

5-55. This paragraph provides troubleshooting procedures in the form of flow charts. These charts, Figures 5-10 through 5-15 provide step-by-step procedures for fault isolation down to active components and critical passive components. In general, these charts are meant as guidelines to logical signal tracing techniques.

5-56. Waveforms keyed to conditions set up by the Troubleshooting charts are also provided; however, as a further aid, waveforms typical of a functioning unit in its normal operating mode are provided on the schematic diagrams which follow the charts. Recommended spares and replaceable parts lists are located in Chapter VI.

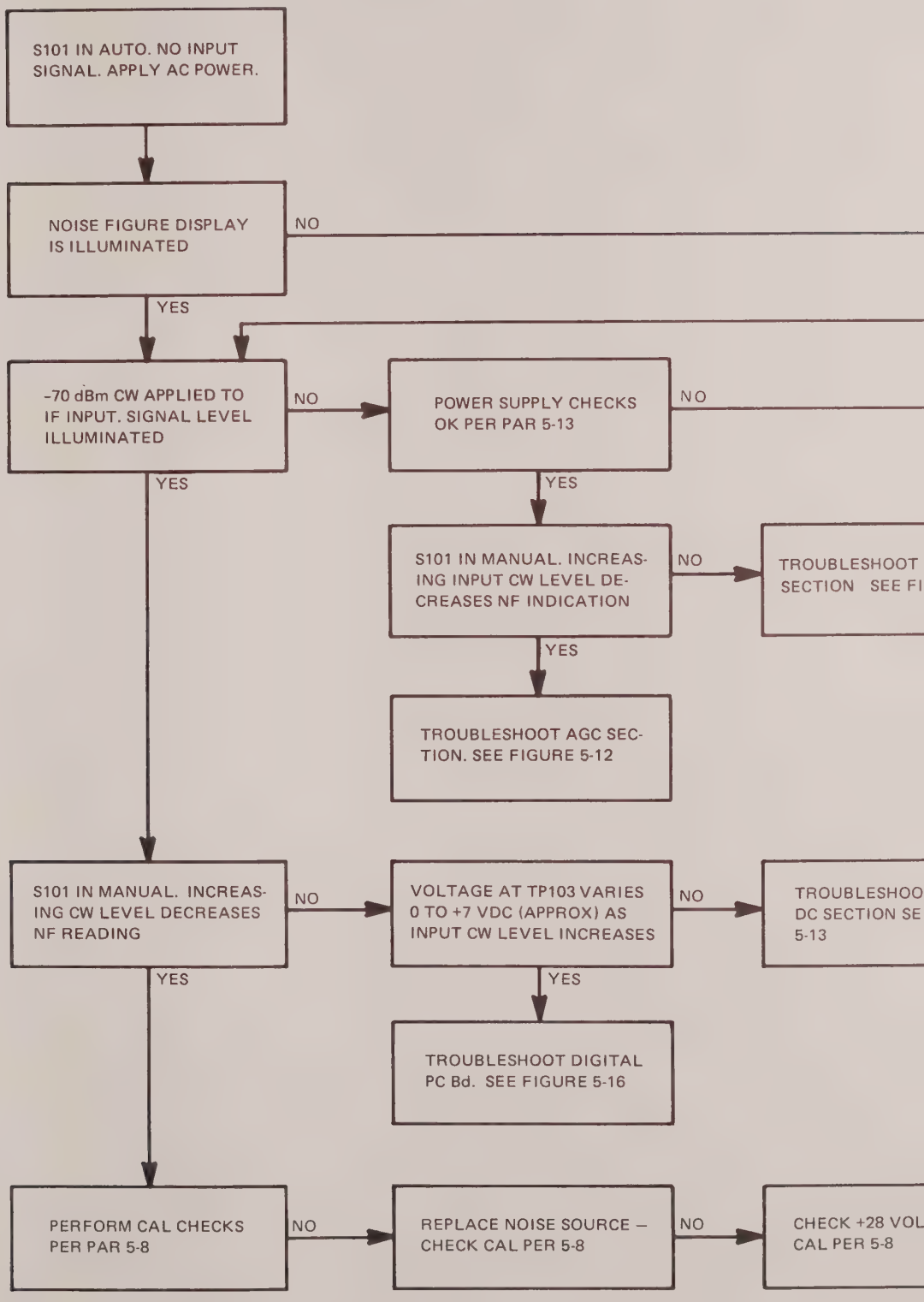
5-57. FACTORY SERVICE

5-58. In the event a difficult service problem occurs, contact your nearest AILTECH Regional Office or Sales Representative by letter, TWX or phone. Please indicate the model number, serial number and specific details of the difficulty involved with as much additional information as you consider necessary to aid in pin-pointing the cure to the problem.

5-59. Should it be necessary to return the equipment to the factory for repair or recalibration, please contact AILTECH or an authorized sales representative in your area before shipping a unit. In your communication arranging for a return, please be sure to include model number, serial number, date of purchase and specific details concerning the problem (in the event of failure) or service desired (in the event of recalibration).

5-60. When an instrument is returned for service, we will proceed to work on the instrument until the charges reach $100. If the total charges exceed $100., an estimate of such charges will be submitted for approval.

5-61. When spare parts are ordered, please indicate a description of the part as well as its part number and also include the model number and serial number of the instrument being repaired.


S101 IN AUTO. NO INPUT SIGNAL. APPLY AC POWER.
NOISE FIGURE DISPLAY IS ILLUMINATED
NO
YES
-70 dBm CW APPLIED TO IF INPUT. SIGNAL LEVEL ILLUMINATED
NO
POWER SUPPLY CHECKS OK PER PAR 5-13
NO
YES
YES
S101 IN MANUAL. INCREASING INPUT CW LEVEL DECREASES NF INDICATION
NO
TROUBLESHOOT
SECTION SEE FI
YES
TROUBLESHOOT AGC SECTION. SEE FIGURE 5-12
S101 IN MANUAL. INCREASING CW LEVEL DECREASES NF READING
NO
VOLTAGE AT TP103 VARIES 0 TO +7 VDC (APPROX) AS INPUT CW LEVEL INCREASES
NO
TROUBLESHOO
DC SECTION SE
5-13
YES
YES
TROUBLESHOOT DIGITAL PC Bd. SEE FIGURE 5-16
PERFORM CAL CHECKS PER PAR 5-8
NO
REPLACE NOISE SOURCE – CHECK CAL PER 5-8
NO
CHECK +28 VOL
CAL PER 5-8

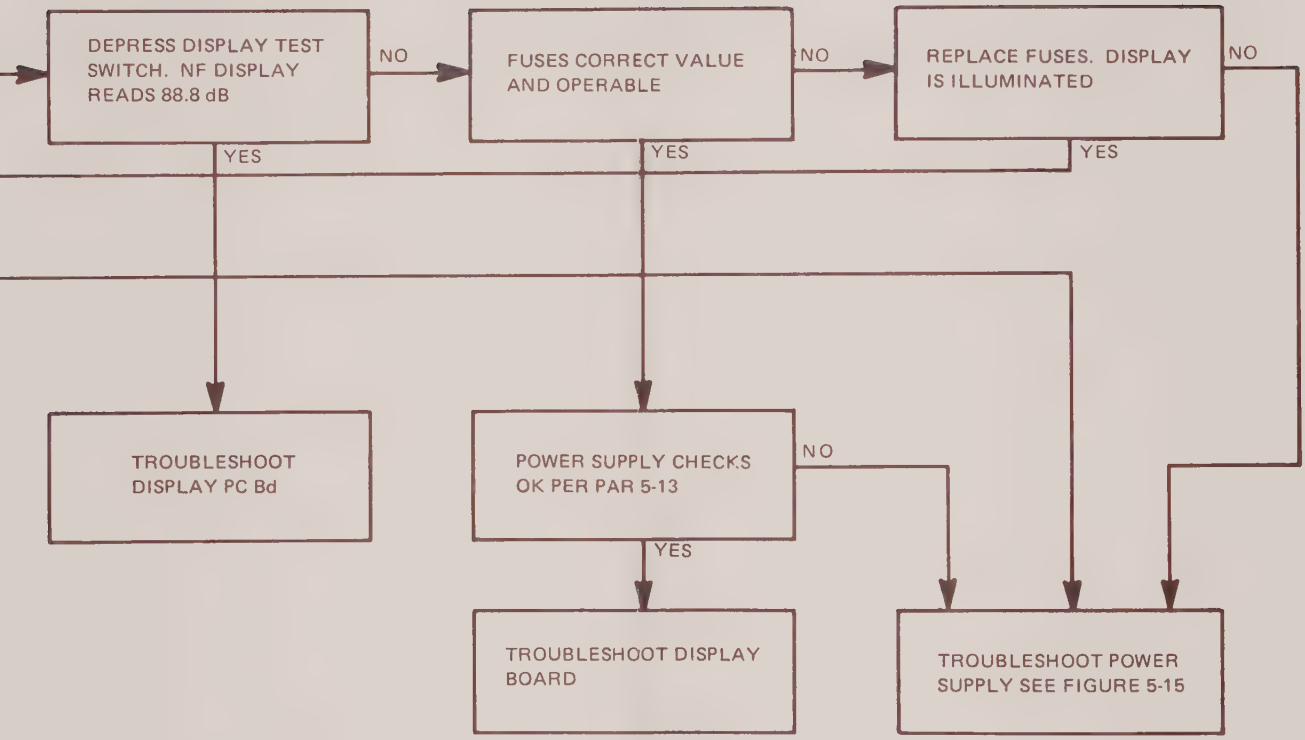
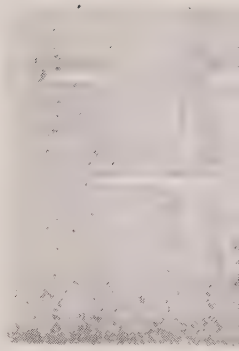
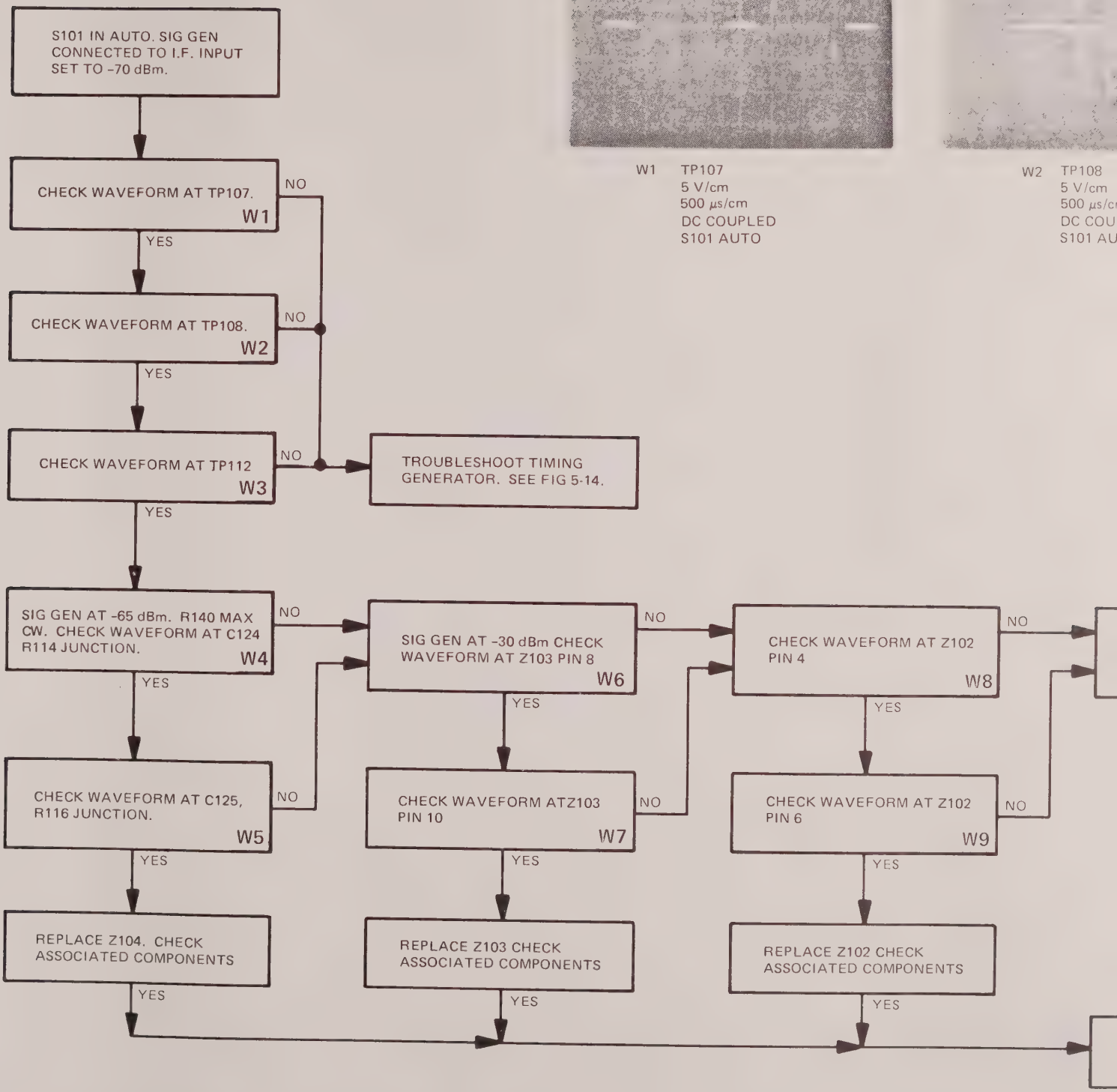


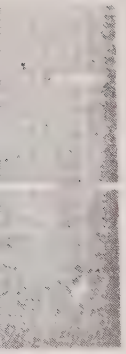
Figure 5-10. General Troubleshooting Chart

W1 TP107
5 V/cm
500 µs/cm
DC COUPLED
S101 AUTO

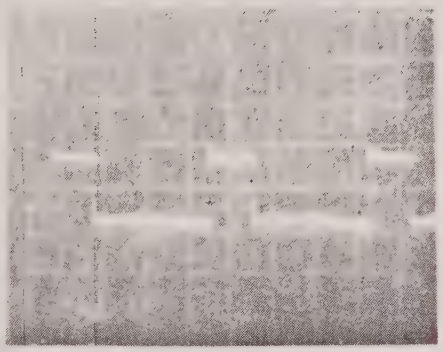


W2 TP108
5 V/cm
500 µs/cm
DC COU
S101 AU

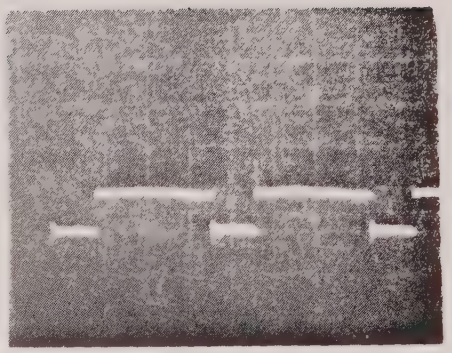




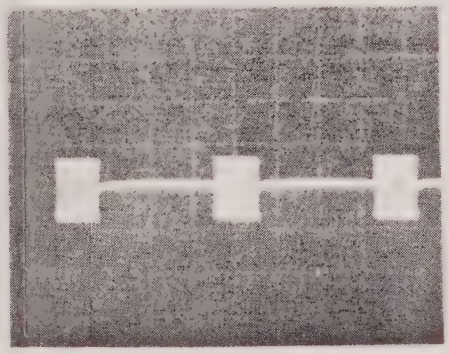
W3 TP112
5 V/cm
500 µs/cm
DC COUPLED
S101 AUTO



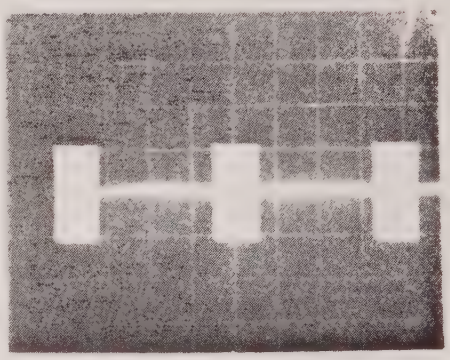
W4 C124, R114 JUNCTION
10m V/cm
500 µs/cm
DC COUPLED
S101 MANUAL
-65 dBM INPUT



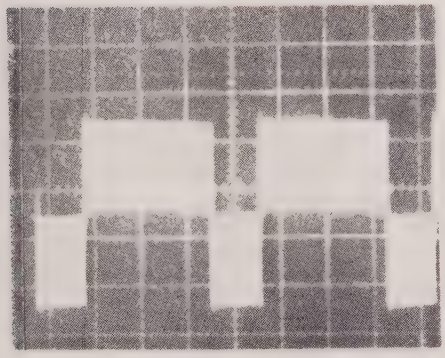
W5 C125, R116 JUNCTION
10 mV/cm
500 µs/cm
DC COUPLED
S101 MANUAL
-65 dBM INPUT



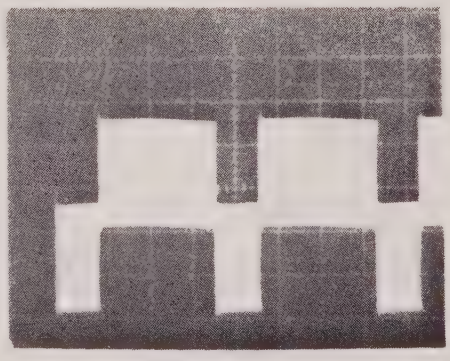
W6 Z103 PIN 8
10m V/cm
500 µs/cm
AC COUPLED
S101 MANUAL
-30 dBM INPUT



W7 Z103 PIN 10
10 mV/cm
500 µs/cm
AC COUPLED
S101 MANUAL
-30 dBM INPUT



W8 Z102 PIN 4
10 mV/cm
500 µs/cm
DC COUPLED
S101 MANUAL
-30 dBM INPUT



W9 Z102 PIN 6
10 mV/cm
500 µs/cm
DC COUPLED
S101 MANUAL
-30 dBM INPUT

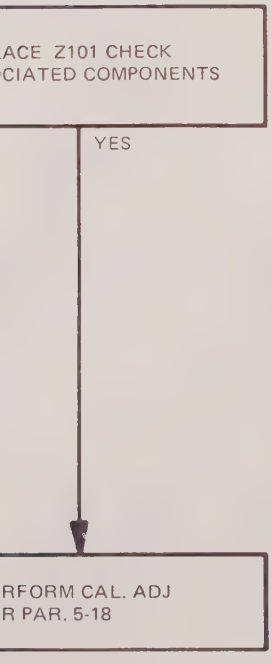
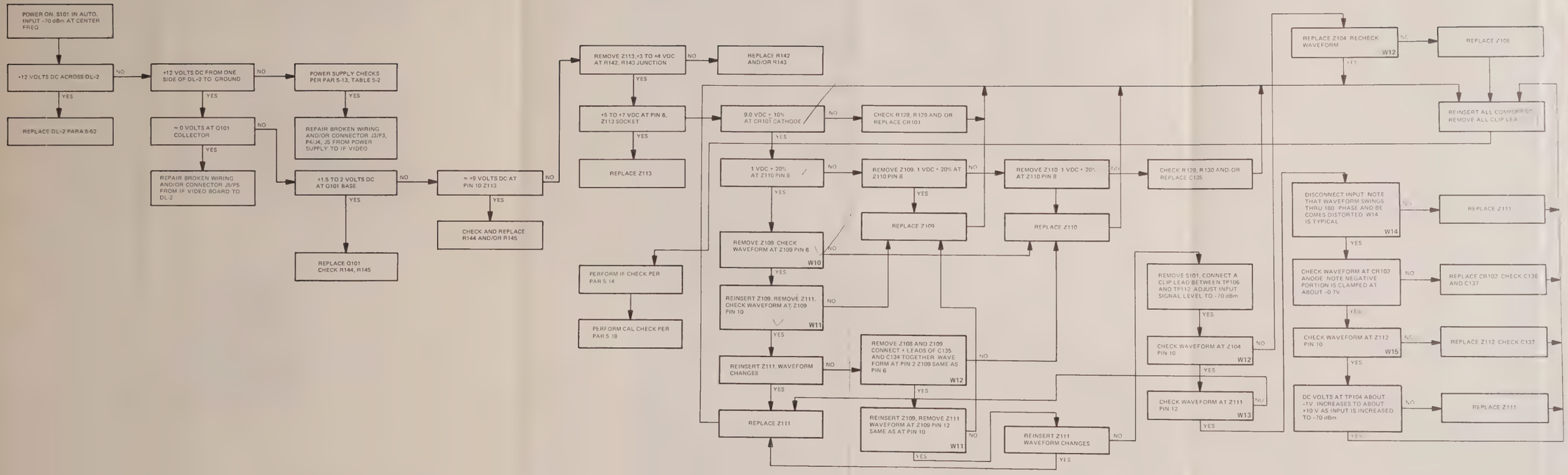


Figure 5-11. IF Troubleshooting Chart


POWER ON. S101 IN AUTO. INPUT -70 dBm AT CENTER FREQ
+12 VOLTS DC ACROSS DL-2
NO
YES
REPLACE DL-2 PARA 5-62
+12 VOLTS DC FROM ONE SIDE OF DL-2 TO GROUND
NO
YES
≈ 0 VOLTS AT Q101 COLLECTOR
NO
YES
REPAIR BROKEN WIRING AND/OR CONNECTOR J5/P5 FROM IF VIDEO BOARD TO DL-2
POWER SUPPLY CHECKS PER PAR 5-13, TABLE 5-2
YES
REPAIR BROKEN WIRING AND/OR CONNECTOR J3/P3, P4/J4, J5 FROM POWER SUPPLY TO IF VIDEO
+1.5 TO 2 VOLTS DC AT Q101 BASE
NO
YES
REPLACE Q101 CHECK R144, R145
≈ +9 VOLTS DC AT PIN 10 Z113
NO
YES
CHECK AND REPLACE R144 AND/OR R145
REMOVE Z113, +3 TO +4 VDC AT R142, R143 JUNCTION
NO
REPLACE R142 AND/OR R143
YES
+5 TO +7 VDC AT PIN 6, Z113 SOCKET
YES
REPLACE Z113
PERFORM IF CHECK PER PAR 5-14
PERFORM CAL CHECK PER PAR 5-18
9.0 VDC ± 10% AT CR101 CATHODE
NO
CHECK R128, R129 AND OR REPLACE CR101
YES
1 VDC ± 20% AT Z110 PIN 8
NO
REMOVE Z109, 1 VDC ± 20% AT Z110 PIN 8
NO
REMOVE Z110, 1 VDC ± 20% AT Z110 PIN 8
NO
CHECK R129, R130 AND OR REPLACE C135
YES
YES
YES
REMOVE Z109, CHECK WAVEFORM AT Z109 PIN 6
W10
NO
REPLACE Z109
REPLACE Z110
YES
REINSERT Z109, REMOVE Z111, CHECK WAVEFORM AT Z109 PIN 10
W11
NO
YES
REINSERT Z111 WAVEFORM CHANGES
NO
REMOVE Z108 AND Z109, CONNECT + LEADS OF C135 AND C134 TOGETHER, WAVE FORM AT PIN 2 Z109 SAME AS PIN 6
W12
NO
YES
YES
REPLACE Z111
REINSERT Z109, REMOVE Z111 WAVEFORM AT Z109 PIN 12 SAME AS AT PIN 10
W11
NO
YES
REINSERT Z111 WAVEFORM CHANGES
NO
YES
REMOVE S101, CONNECT A CLIP LEAD BETWEEN TP106 AND TP112, ADJUST INPUT SIGNAL LEVEL TO -70 dBm
YES
CHECK WAVEFORM AT Z104 PIN 10
W12
NO
YES
CHECK WAVEFORM AT Z111 PIN 12
W13
NO
YES
REPLACE Z104, RECHECK WAVEFORM
W12
NO
REPLACE Z108
YES
REINSERT ALL COMPONENTS, REMOVE ALL CLIP LEA
DISCONNECT INPUT. NOTE THAT WAVEFORM SWINGS THRU 180° PHASE AND BECOMES DISTORTED. W14 IS TYPICAL
W14
NO
REPLACE Z111
YES
CHECK WAVEFORM AT CR102 ANODE. NOTE NEGATIVE PORTION IS CLAMPED AT ABOUT -0.7V
NO
REPLACE CR102, CHECK C136 AND C137
YES
CHECK WAVEFORM AT Z112 PIN 10
W15
NO
REPLACE Z112, CHECK C137
YES
DC VOLTS AT TP104 ABOUT -1V INCREASES TO ABOUT +10 V AS INPUT IS INCREASED TO -70 dBm
NO
REPLACE Z111
YES

W10 Z109 PIN 6
0.5 V/cm
500 μs/cm
DC COUPLED

W11 Z109 PIN 10
500 μs/cm
DC COUPLED

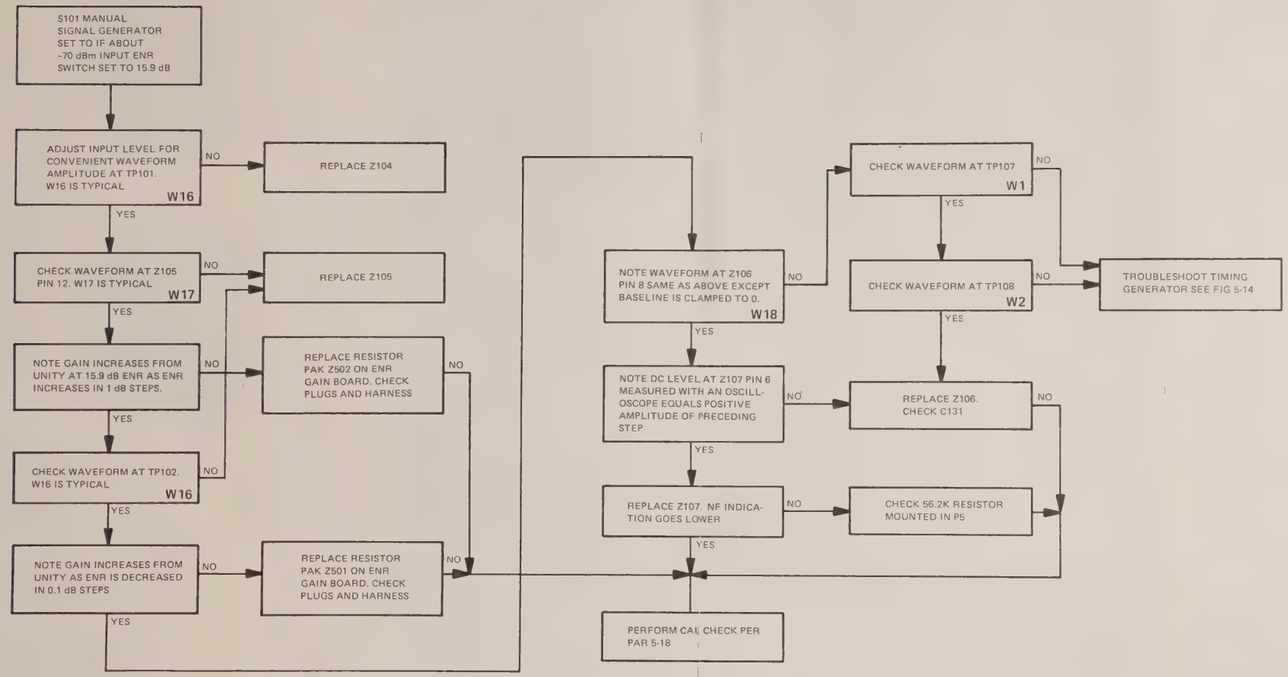
W12 Z104 PIN 10
2 V/cm
500 μs/cm
DC COUPLED
S101 REMOVED
TP106 CONNECTED TO TP112

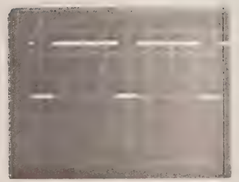
W13 Z111 PIN 12
5 V/cm
500 μs/cm
DC COUPLED
S101 REMOVED
TP106 CONNECTED TO TP112

W14 Z111 PIN 12
5 V/cm
500 μs/cm
DC COUPLED
S101 REMOVED
TP106 CONNECTED TO TP112, NO INPUT

W15 Z112 PIN 10
0.2 V/cm
500 μs/cm
DC COUPLED
S101 REMOVED
TP106 CONNECTED TO TP112, NO INPUT

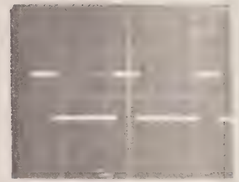
Figure 5-12. AGC Troubleshooting Chart





W1 TP107
5 V/cm
500 µs/cm
DC COUPLED
S101 AUTO

W2 TP108
5 V cm
500 µs cm
DC COUPLED
S101 AUTO

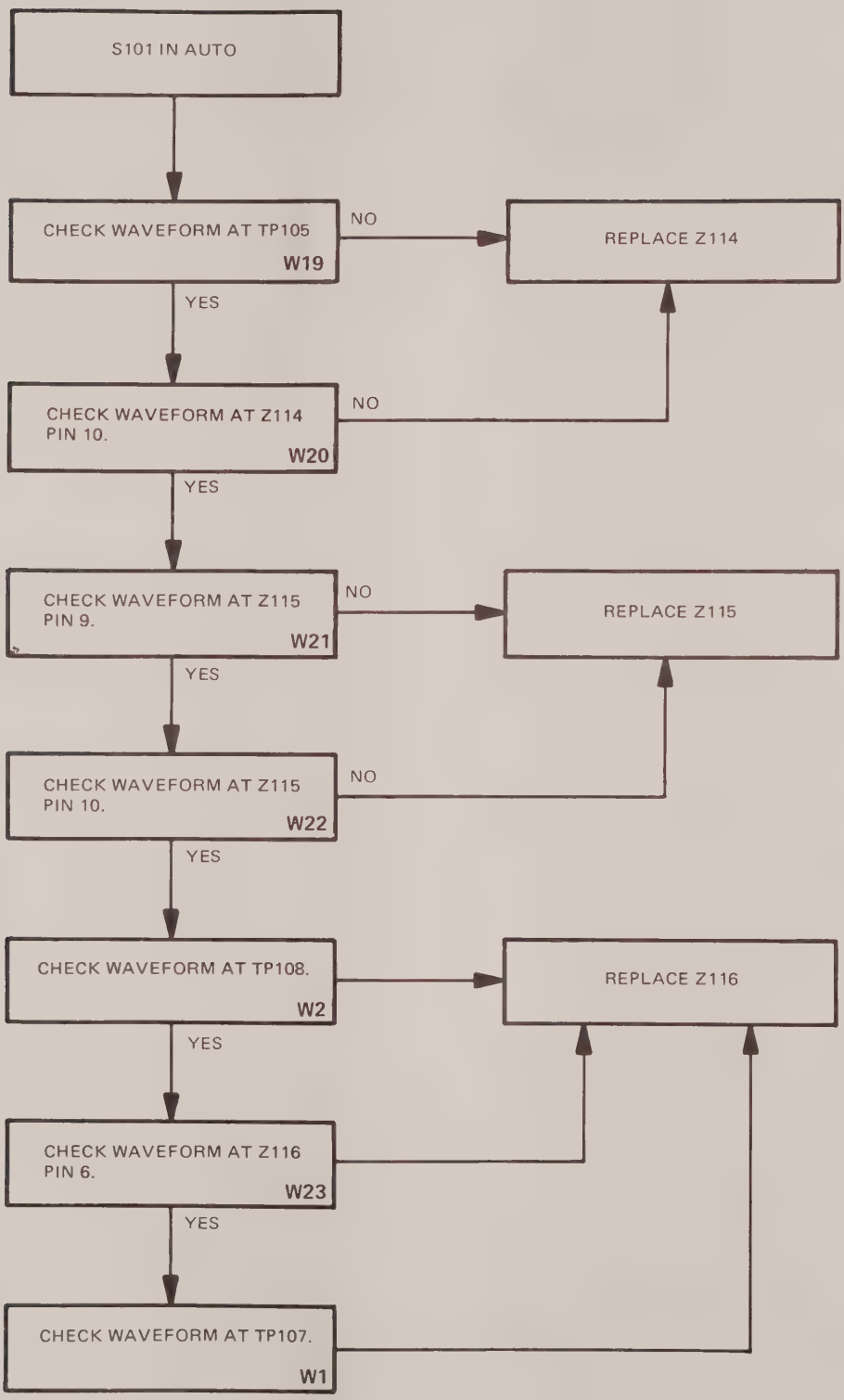


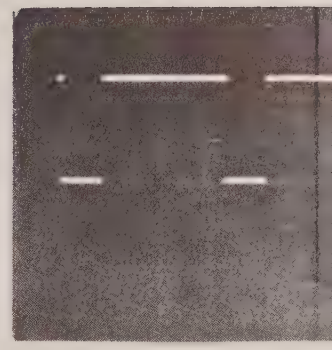
W16 TP 101, 102 TYPICAL
0.2 V/cm
500 µs/cm
DC COUPLED – OFFSET
S101 MANUAL

W17 Z105 PIN 12 TYPICAL
0.2 V/cm
500 µs/cm
DC COUPLED – OFFSET
S101 MANUAL

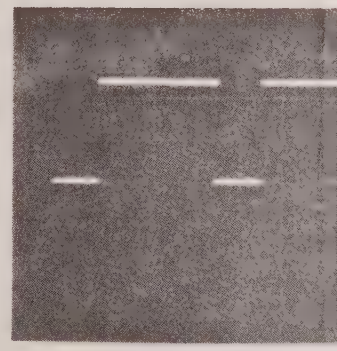
W18 Z106 PIN 8 TYPICAL
2 V cm
500 µs/cm
DC COUPLED
S101 MANUAL

Figure 5-13. Video-DC Troubleshooting Chart

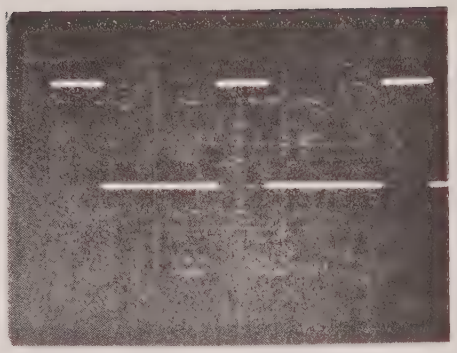




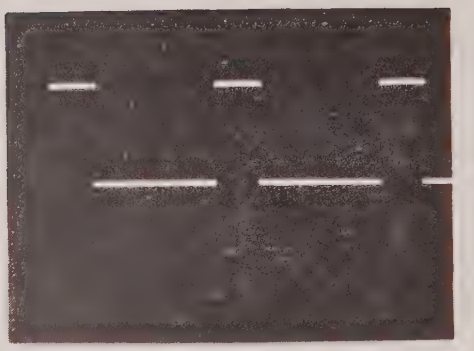
W1 TP107
5 V/cm
500 µs/cm
DC COUPLED
S101 AUTO



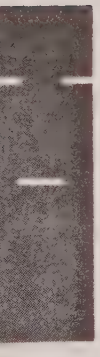
W20 Z114 PIN 10
5 V/cm
500 µs/cm
DC COUPLED

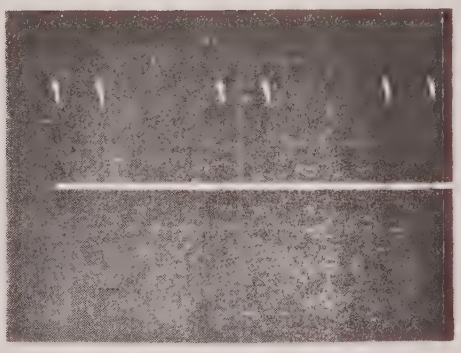


W2 TP108
5 V/cm
500 μs/cm
DC COUPLED
S101 AUTO

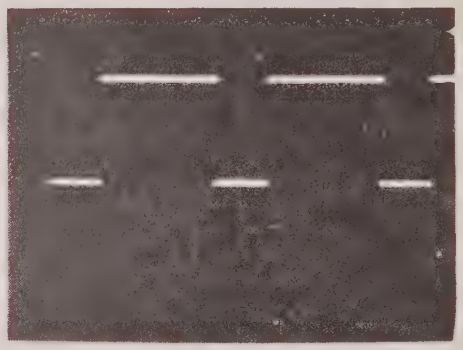


W19 TP105
5 V/cm
500 μs/cm
DC COUPLED





W21 Z115 PIN 9
5 V/cm
500 μs/cm
DC COUPLED



W22 Z115 PIN 10
5 V/cm
500 μs/cm
DC COUPLED

W23 Z116 PIN 6
5 V/cm
500 μs/cm
DC COUPLED

Figure 5-14. Timing Generator Troubleshooting Chart

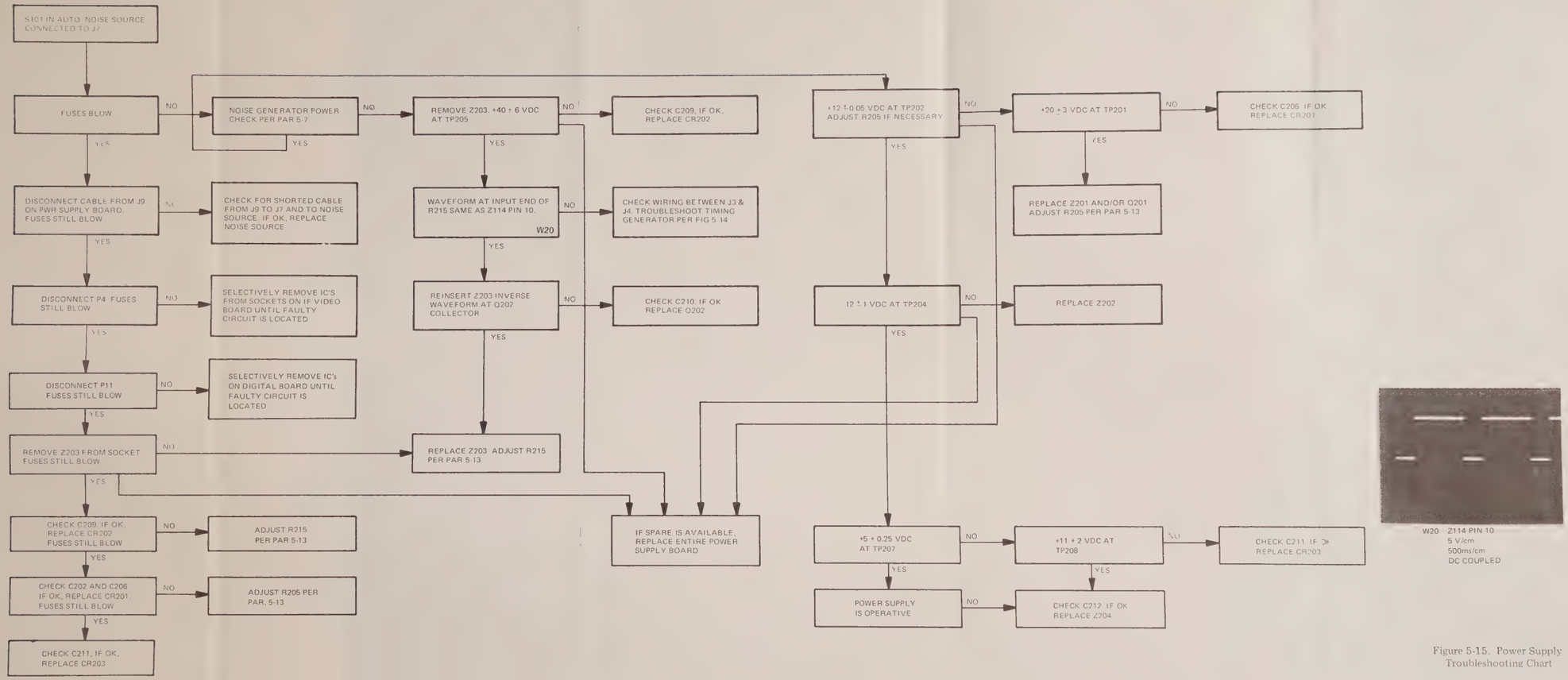
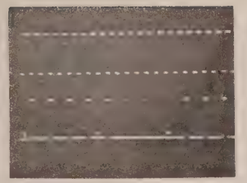
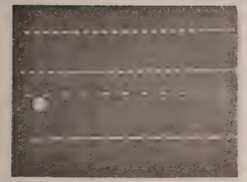

S101 IN AUTO, NOISE SOURCE CONNECTED TO J7
FUSES BLOW
NO
YES
NOISE GENERATOR POWER CHECK PER PAR 5-7
NO
YES
REMOVE Z203, +40 ± 6 VDC AT TP205
NO
YES
CHECK C209, IF OK, REPLACE CR202
+12 ± 0.05 VDC AT TP202 ADJUST R205 IF NECESSARY
NO
YES
+20 ± 3 VDC AT TP201
NO
YES
CHECK C206 IF OK REPLACE CR201
DISCONNECT CABLE FROM J9 ON PWR SUPPLY BOARD. FUSES STILL BLOW
NO
YES
CHECK FOR SHORTED CABLE FROM J9 TO J7 AND TO NOISE SOURCE. IF OK, REPLACE NOISE SOURCE
WAVEFORM AT INPUT END OF R215 SAME AS Z114 PIN 10.
W20
NO
YES
CHECK WIRING BETWEEN J3 & J4. TROUBLESHOOT TIMING GENERATOR PER FIG 5-14
REPLACE Z201 AND/OR Q201 ADJUST R205 PER PAR 5-13
DISCONNECT P4 FUSES STILL BLOW
NO
YES
SELECTIVELY REMOVE IC'S FROM SOCKETS ON IF VIDEO BOARD UNTIL FAULTY CIRCUIT IS LOCATED
REINSERT Z203 INVERSE WAVEFORM AT Q202 COLLECTOR
NO
YES
CHECK C210, IF OK REPLACE Q202
12 ± 1 VDC AT TP204
NO
YES
REPLACE Z202
DISCONNECT P11 FUSES STILL BLOW
NO
YES
SELECTIVELY REMOVE IC's ON DIGITAL BOARD UNTIL FAULTY CIRCUIT IS LOCATED
REMOVE Z203 FROM SOCKET FUSES STILL BLOW
NO
YES
REPLACE Z203 ADJUST R215 PER PAR 5-13
CHECK C209, IF OK, REPLACE CR202 FUSES STILL BLOW
NO
YES
ADJUST R215 PER PAR 5-13
CHECK C202 AND C206 IF OK, REPLACE CR201. FUSES STILL BLOW
NO
YES
ADJUST R205 PER PAR. 5-13
CHECK C211, IF OK, REPLACE CR203
IF SPARE IS AVAILABLE, REPLACE ENTIRE POWER SUPPLY BOARD
+5 ± 0.25 VDC AT TP207
NO
YES
+11 ± 2 VDC AT TP208
NO
YES
CHECK C211 IF OK REPLACE CR203
POWER SUPPLY IS OPERATIVE
NO
CHECK C212 IF OK REPLACE Z204
W20 Z114 PIN 10
5 V/cm
500ms/cm
DC COUPLED

Figure 5-15. Power Supply Troubleshooting Chart

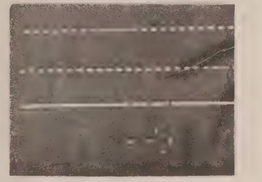
W25 TP304
2 V/cm
1 µs/cm
INT TRIGGER
DC COUPLED



W26 Z308-5 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR F < 3.3 db

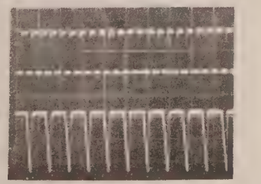


W27 Z315-12 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED



W28 Z304-9 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR F < 3.3 db

W29 Z316-8 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED



W30 TP303, (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED

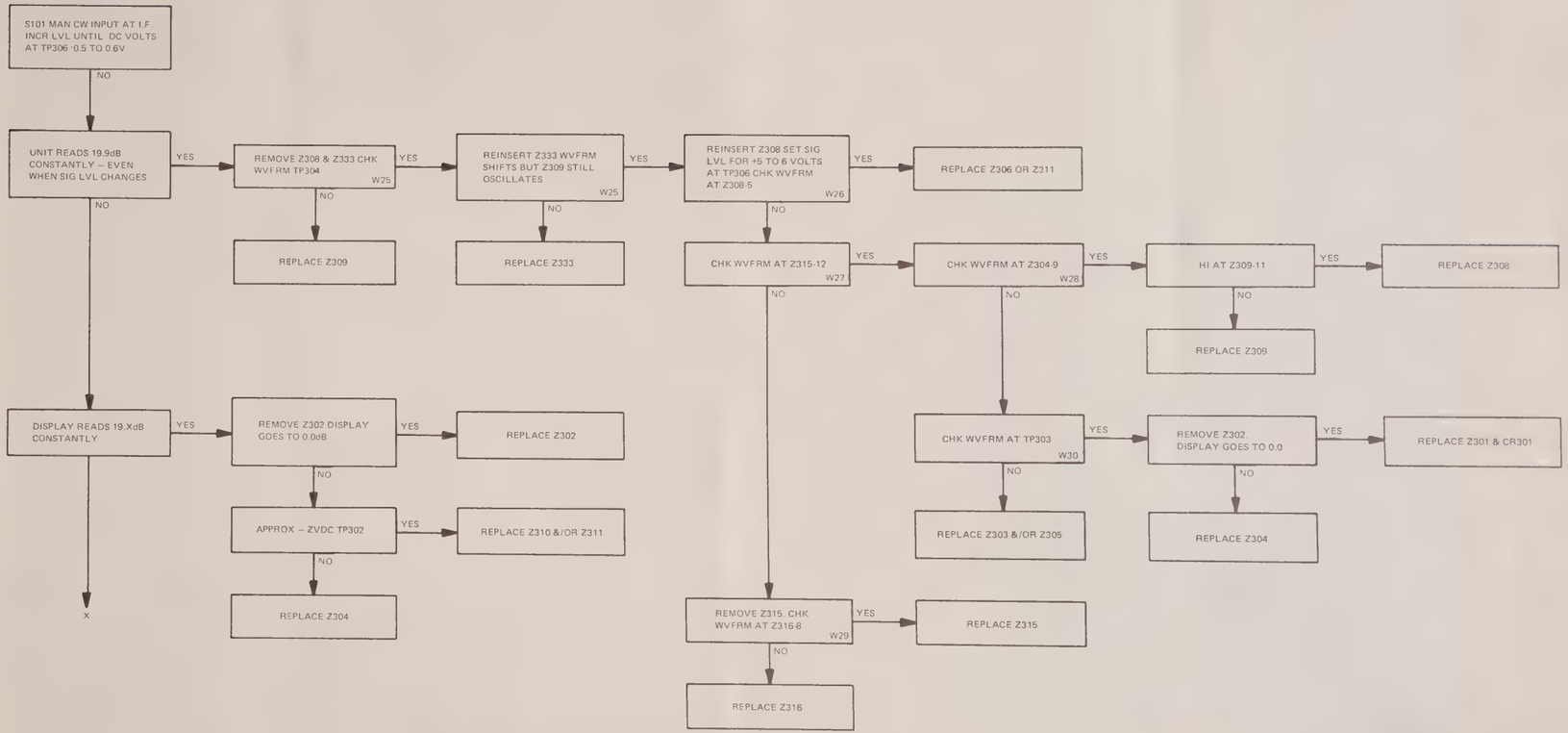
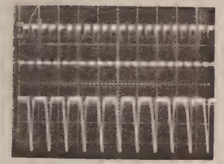
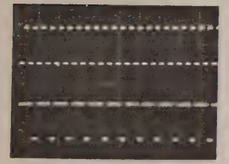


Figure 5-16. Digital/Display Troubleshooting Chart (Part 1)

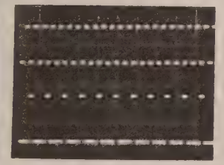
W26 Z308-5 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR F <3.3 db



W30 TP303, (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED



W31 Z312-11 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED



W32 Z308-9 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED

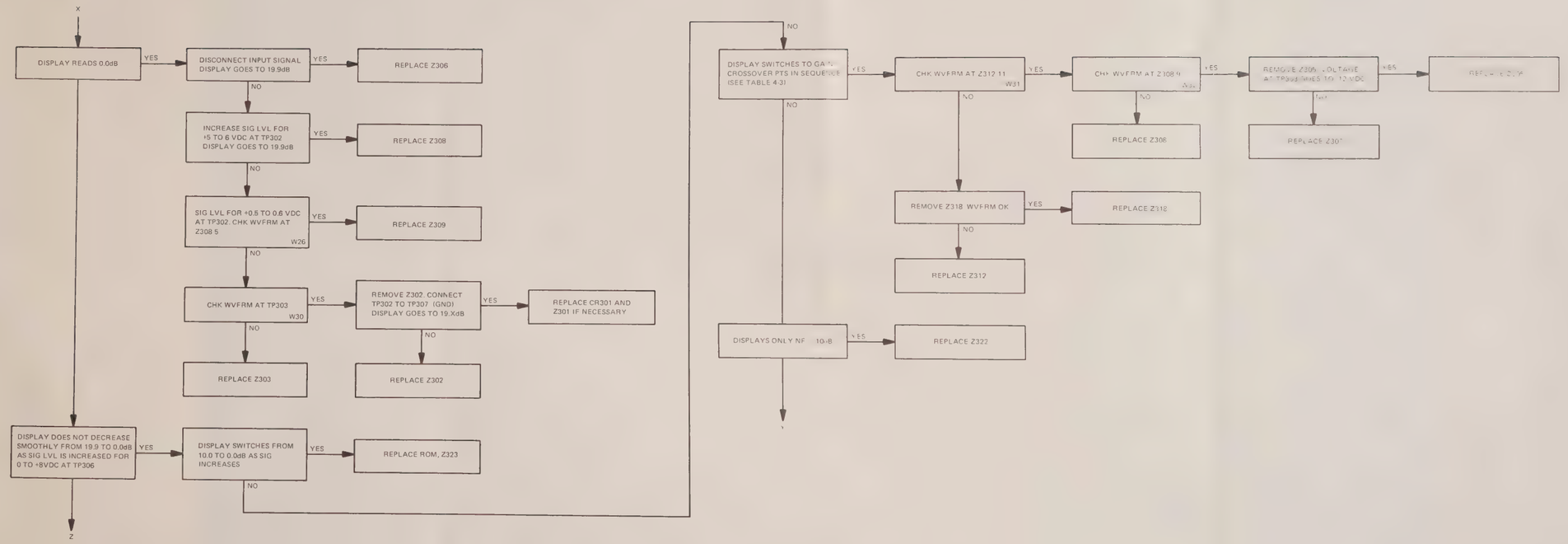
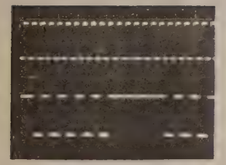
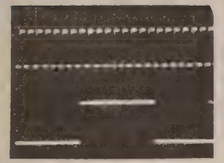


Figure 5-16. Digital/Display Troubleshooting Chart (Part 2)

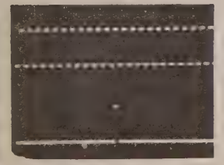


W33 Z314-8 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR 0.0 db DISPLAY

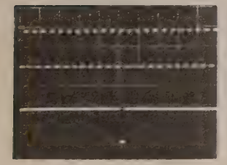


W34 Z314-12 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR 0.0 db DISPLAY

W35 TP301
2 V/cm
500 µs/cm
Z315-12 TRIGGER
DC COUPLED



W36 TP305 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED



W37 Z317-8 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED

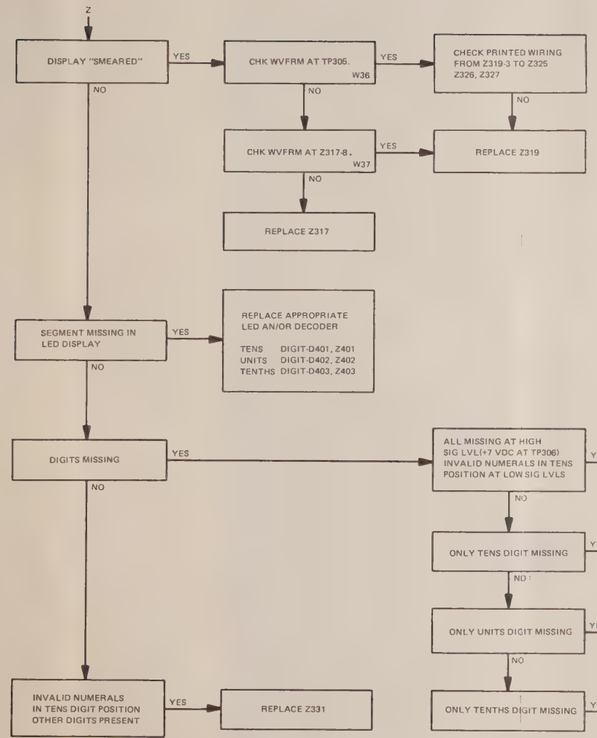


Figure 5-16. Digital/Display Troubleshooting Chart (Part 3)

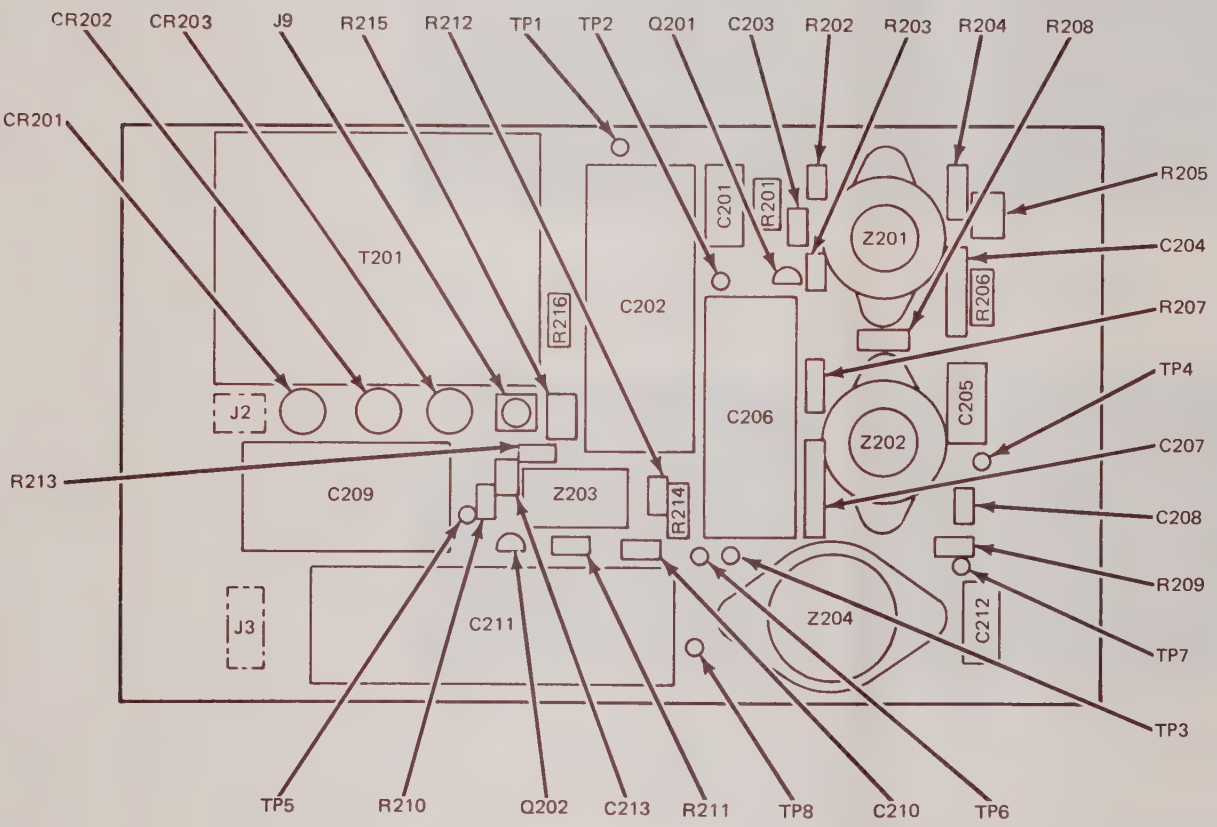
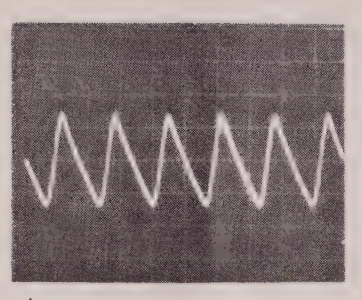
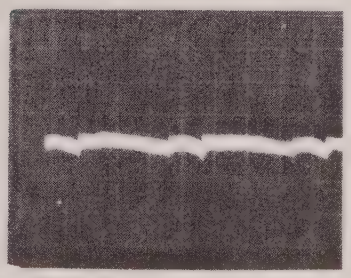


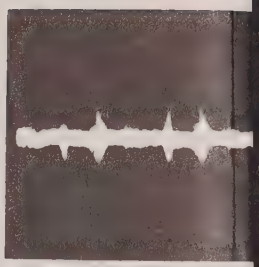
Figure 5-17. Power Supply, Parts Location and Schematic Diagrams
(Part 1 of 2)



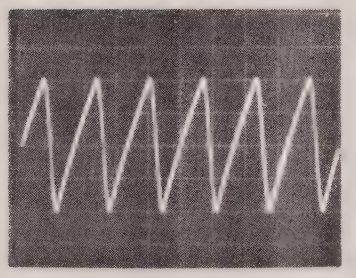
1
TP201
0.2 V/cm
5 ms/cm
LINE TRIGGER
AC COUPLED



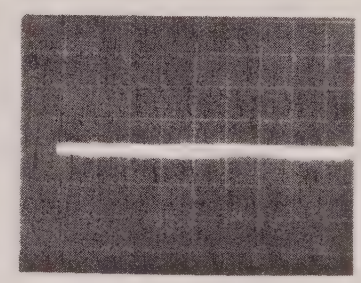
2
TP202
2m V/cm
1 ms/cm
AC COUPLED



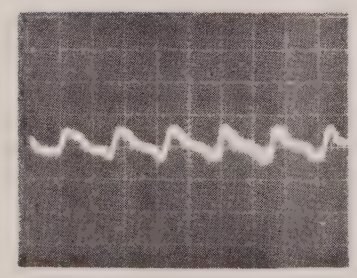
7
TP207
2m V/cm
5 ms/cm
LINE TRIGG
AC COUPLED



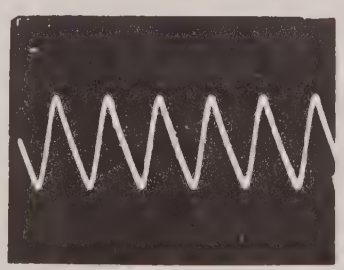
3
TP203
0.2 V/cm
5 ms/cm
LINE TRIGGER
AC COUPLED



4
TP204
2m V/cm
1 ms/cm
AC COUPLED



5
TP205
0.1 V/cm
5 ms/cm
LINE TRIGGER
AC COUPLED



6
TP208
0,2 V/cm
5 ms/cm
LINE TRIGGER
AC COUPLED

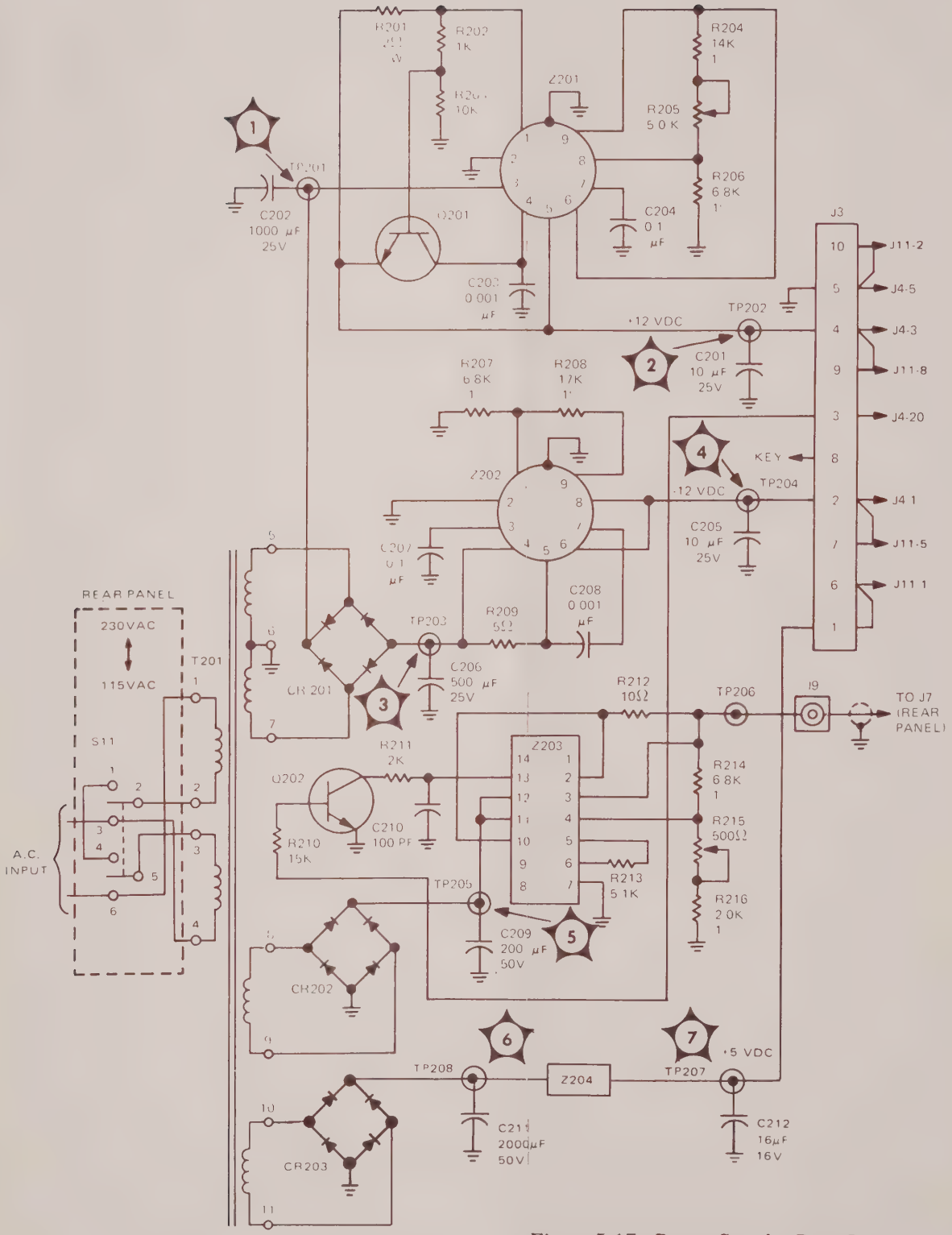
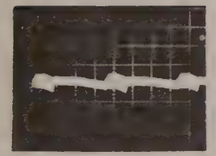
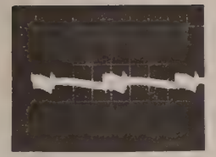


Figure 5-17. Power Supply, Parts Location and Schematic Diagrams (Part 2 of 2)



9 Z102 PIN 8
10m V/cm
0.5 µs/cm
AC COUPLED
AUTO NF 3dB



10 Z103 PIN 10
5 mV/cm
0.5 µs/cm
AC COUPLED
AUTO NF 3dB

11 TP101
0.2 V/cm
0.5 µs/cm
DC COUPLED
AUTO NF 3dB

12 Z105 PIN 12
0.2 V/cm
0.5 µs/cm
DC COUPLED
AUTO NF 3dB
ENR SET 15.5 dB

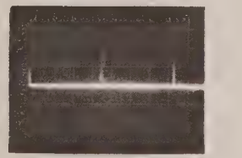
13 TP102
0.2 V/cm
0.5 µs/cm
DC COUPLED
AUTO NF 3dB
ENR SET 15.5 dB

14 Z104 PIN 10
1 V/cm
0.5 µs/cm
DC COUPLED
AUTO NF 3dB

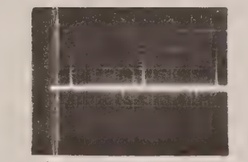
15 Z106 PIN 10
0.2 V/cm
0.5 µs/cm
DC COUPLED
AUTO NF 3dB
ENR SET 15.5 dB

16 Z114 PIN 4
5 V/cm
0.5 µs/cm
DC COUPLED

17 TP106
5 V/cm
0.5 µs/cm
DC COUPLED

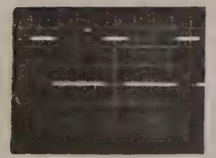


18 Z115 PIN 5
5 V/cm
0.5 µs/cm
DC COUPLED

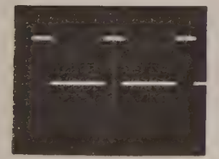


19 Z115 PIN 4
5 V/cm
0.5 µs/cm
DC COUPLED

20 TP107
5 V/cm
0.5 µs/cm
DC COUPLED
S101 AUTO



21 TP108
5 V/cm
0.5 µs/cm
DC COUPLED
S101 AUTO

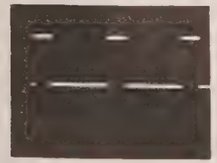


22 TP105
5 V/cm
0.5 µs/cm
DC COUPLED

23 Z114 PIN 10
5 V/cm
0.5 µs/cm
DC COUPLED

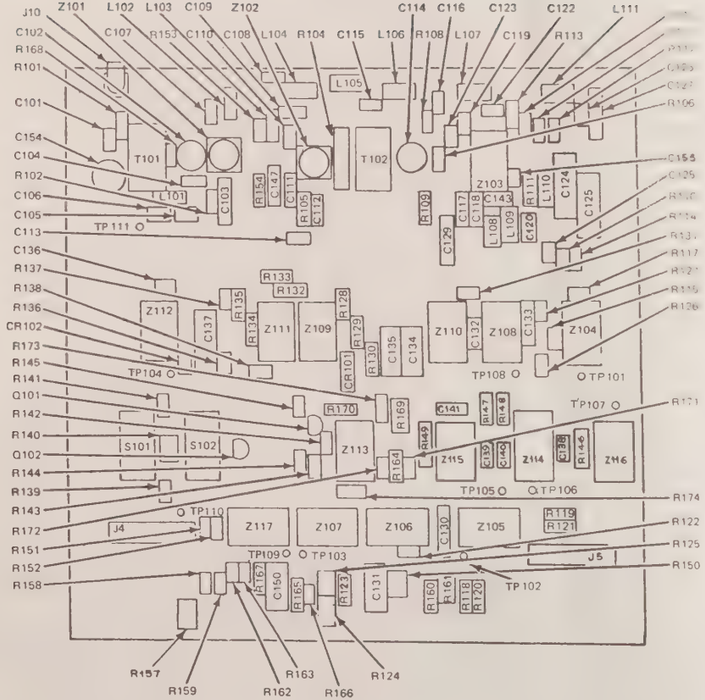
24 Z115 PIN 9
5 V/cm
0.5 µs/cm
DC COUPLED

25 Z115 PIN 10
5 V/cm
0.5 µs/cm
DC COUPLED



26 Z116 PIN 6
5 V/cm
0.5 µs/cm
DC COUPLED

Figure 5-18. IF-Video Parts Location and Schematic Diagrams (Part 1 of 2)



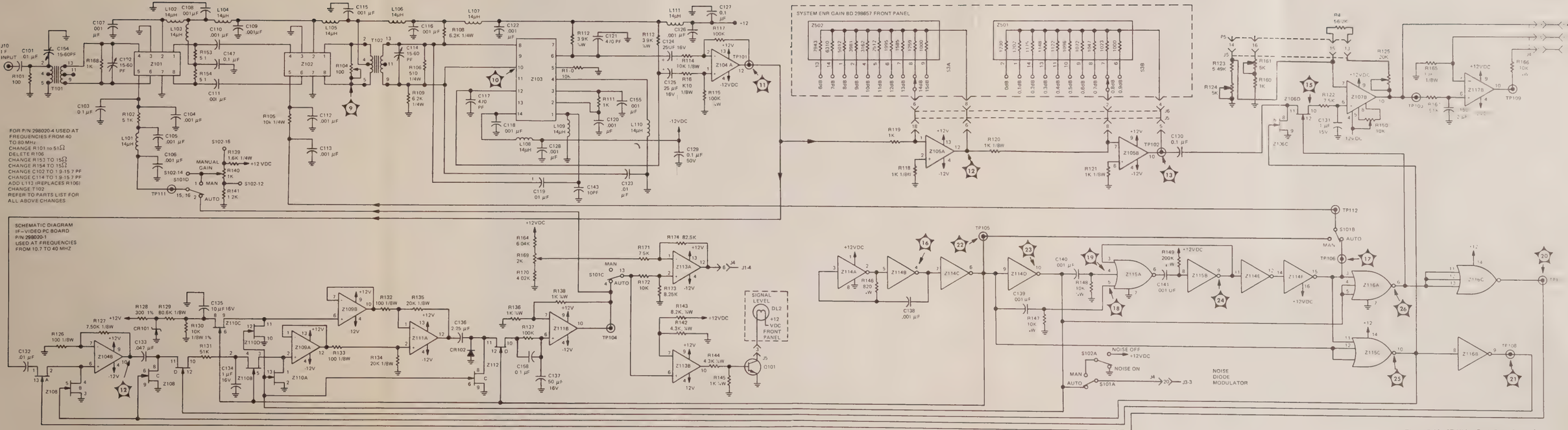
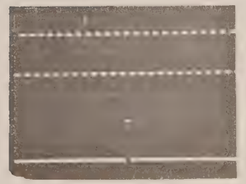


Figure 5-18. IF-Video Parts Location and Schematic Diagrams (Part 2 of 2)

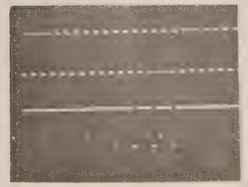
W27 TP301
2 V/cm
500 µs/cm
Z315-12 TRIGGER
DC COUPLED

W29 TP302 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR F<3.3 dB



W30 TP305 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED

W31 TP304
2 V/cm
1 µs/cm
INT TRIGGER
DC COUPLED



W32 Z304-9 (TP301 REF)
2 V/cm
2 ms/cm
Z315-12 TRIGGER
DC COUPLED
TYPICAL FOR F<3.3 dB

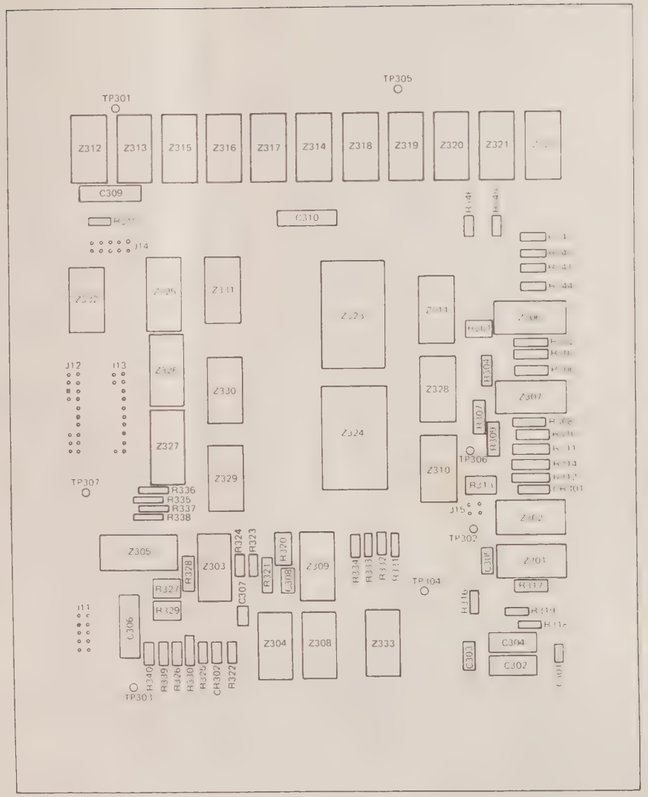


Figure 5-19. Digital Board Parts Location and Schematic Diagram (Part 1)

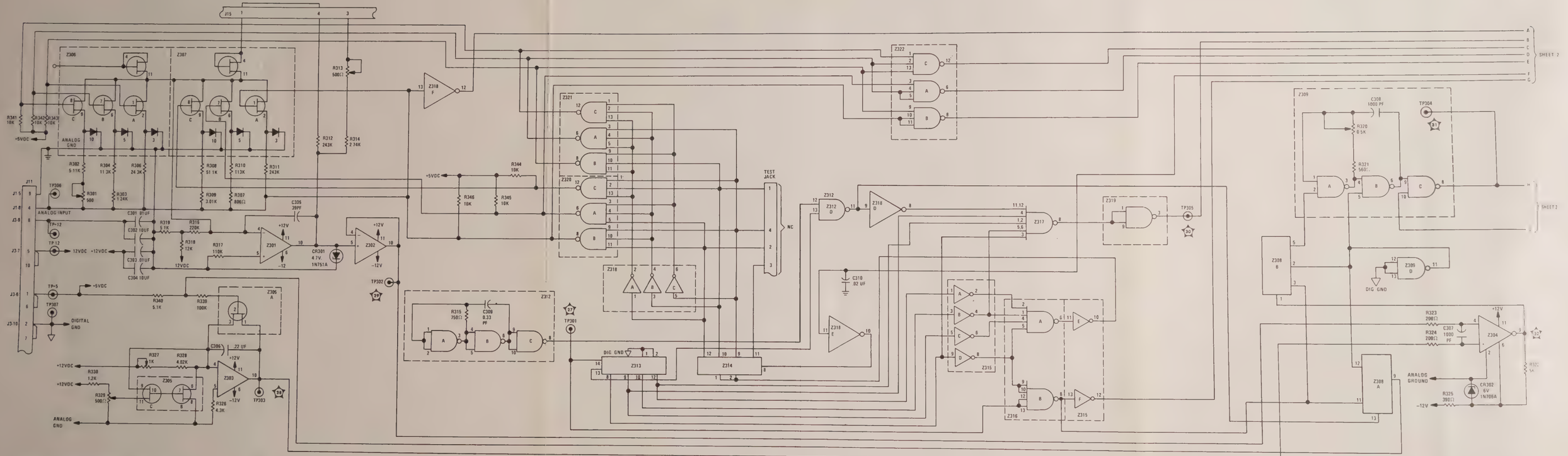


Figure 5-19. Digital Board Parts Location and Schematic Diagram (Part 2)

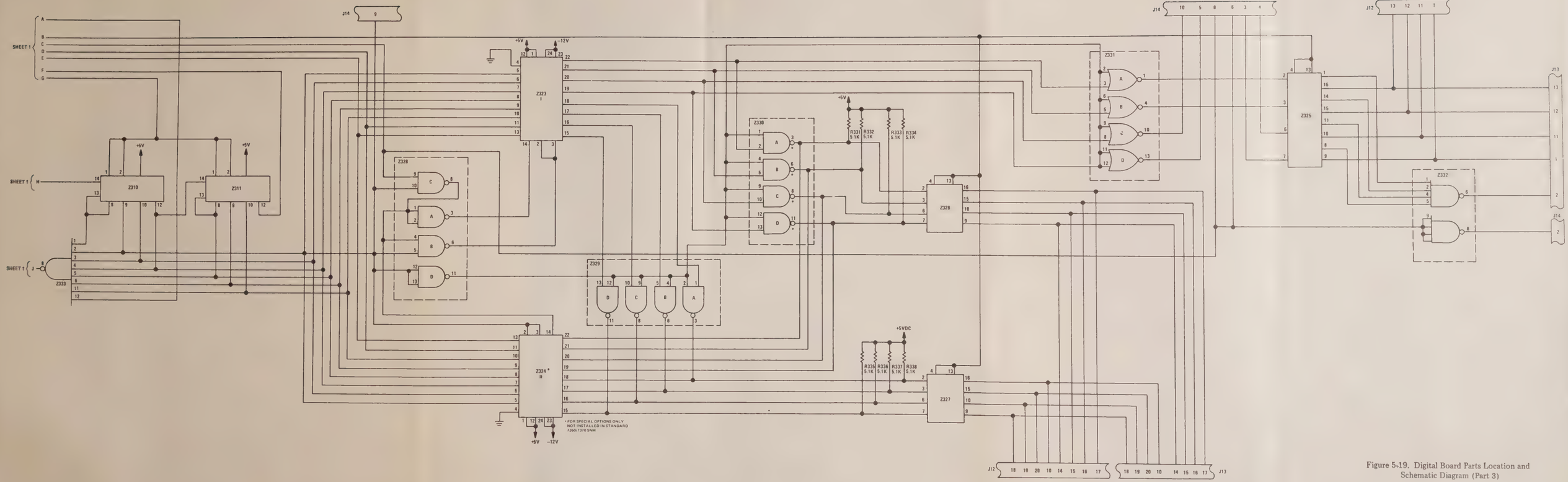


Figure 5-19. Digital Board Parts Location and Schematic Diagram (Part 3)

D401
D402
DA03
1401
1402
R401
R402
R403
R404
R405
R406
R407
R408
R409
R410
R411
R412
R413
R414
R415
R416
R417
R418
R419
R420
R421
R422
R423
R424
Z401
Z402
Z403

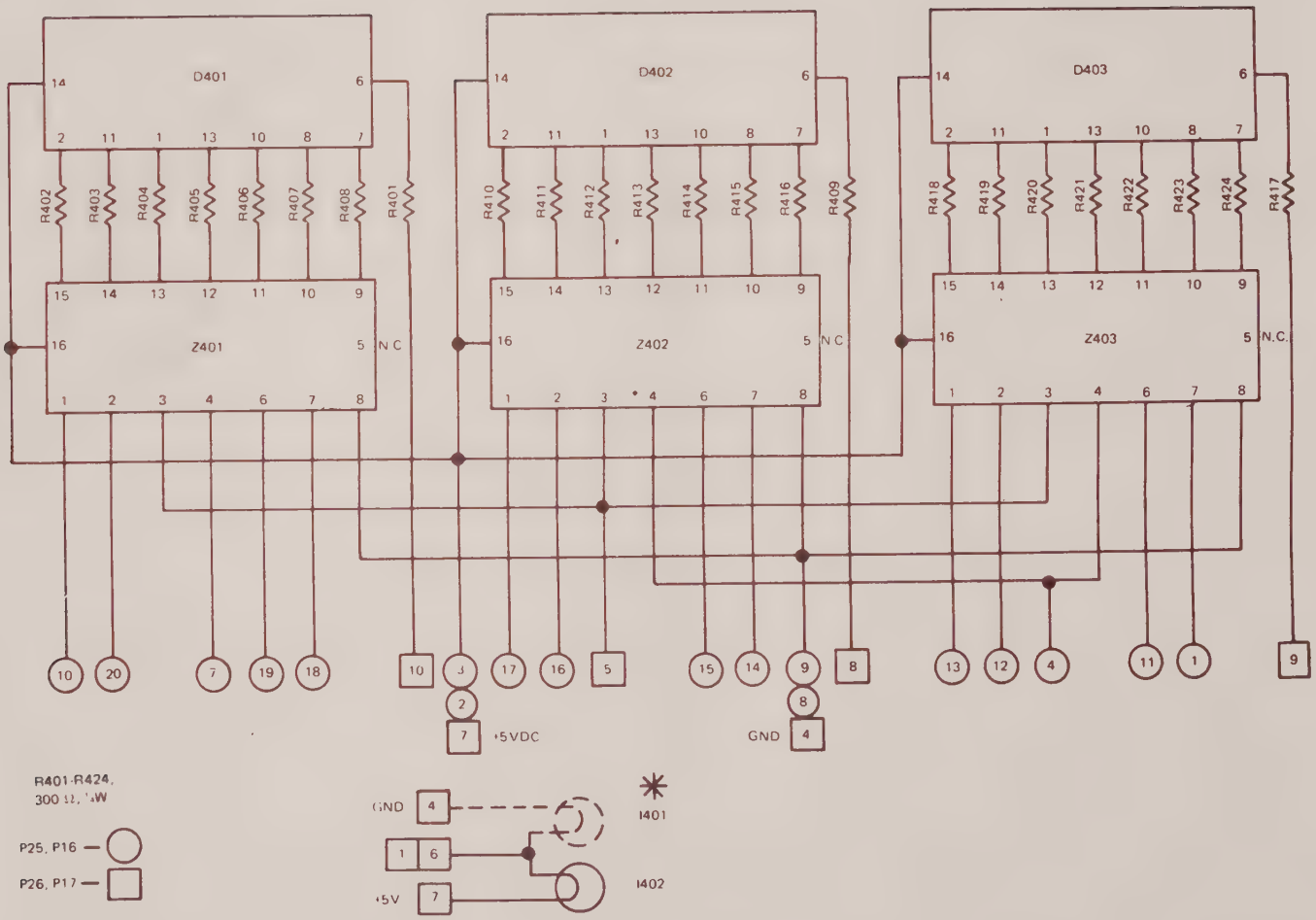
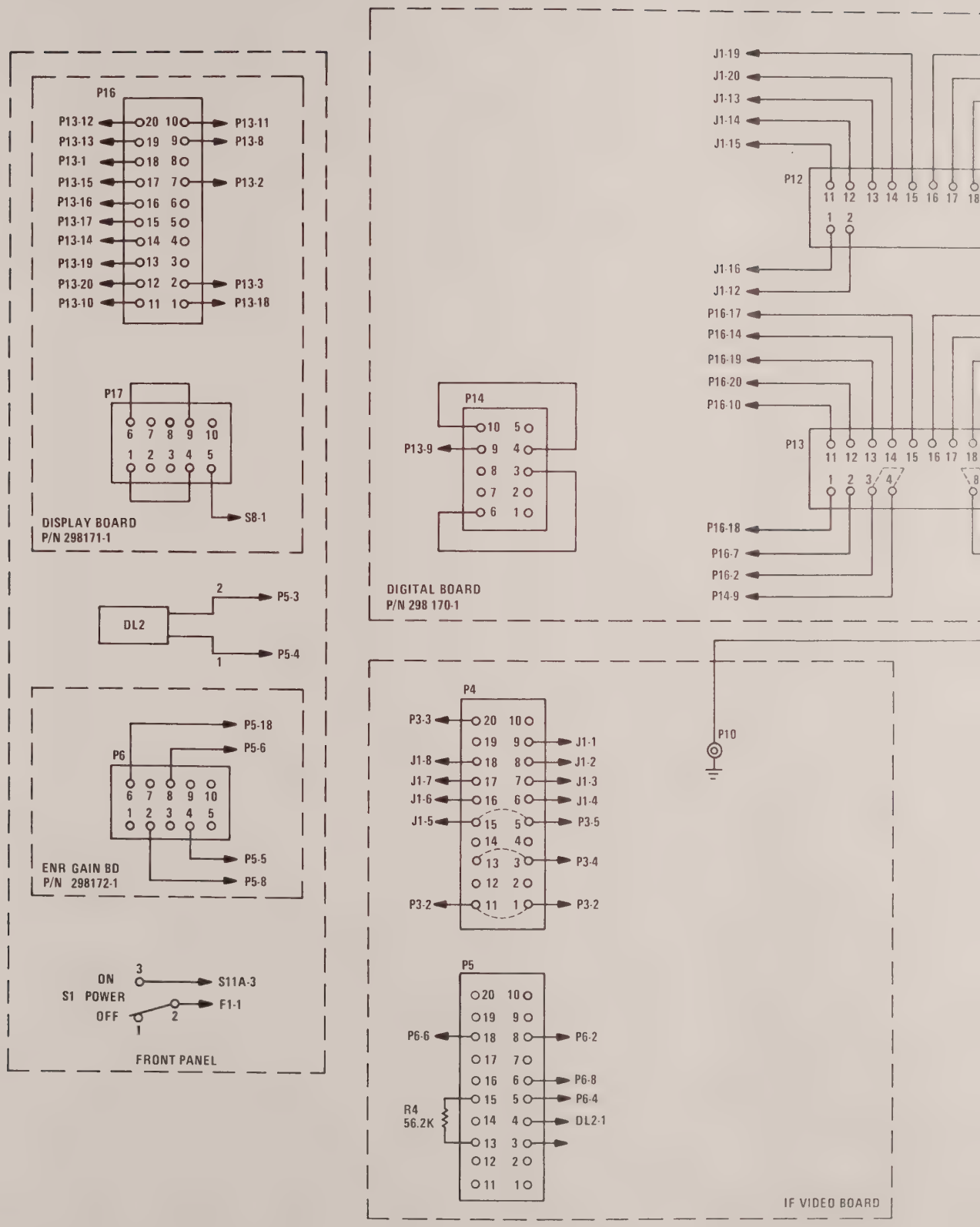
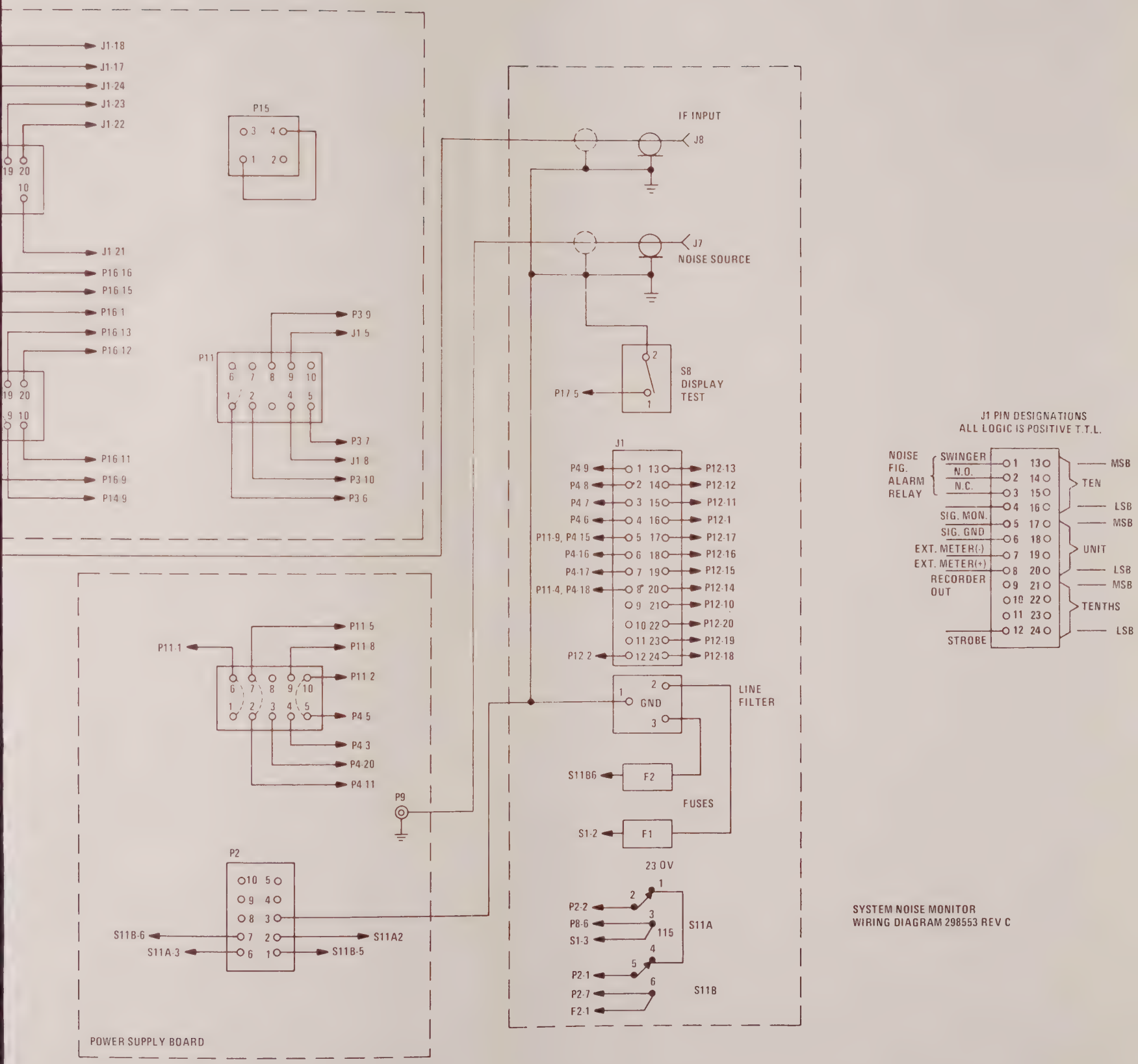


Figure 5-20. Display Parts Location and Schematic Diagram


P16
P13-12
P13-13
P13-1
P13-15
P13-16
P13-17
P13-14
P13-19
P13-20
P13-10
P13-11
P13-8
P13-2
P13-3
P13-18
P17
S8-1
DISPLAY BOARD
P/N 298171-1
DL2
P5-3
P5-4
P6
P5-18
P5-6
P5-5
P5-8
ENR GAIN BD
P/N 298172-1
S1 POWER
ON
OFF
S11A-3
F1-1
FRONT PANEL
P14
P13-9
J1-19
J1-20
J1-13
J1-14
J1-15
P12
J1-16
J1-12
P16-17
P16-14
P16-19
P16-20
P16-10
P13
P16-18
P16-7
P16-2
P14-9
DIGITAL BOARD
P/N 298 170-1
P10
P4
P3-3
J1-8
J1-7
J1-6
J1-5
P3-2
J1-1
J1-2
J1-3
J1-4
P3-5
P3-4
P3-2
P5
P6-6
R4
56.2K
P6-2
P6-8
P6-4
DL2-1
IF VIDEO BOARD



SYSTEM NOISE MONITOR
WIRING DIAGRAM 298553 REV C

Figure 5-21. Wiring Diagram

CHAPTER VI

SPARE PARTS

6-1. GENERAL

The System Noise Monitor is intended to be maintained by the replacement of defective modules. All subassemblies are modularized and easily replaceable, by design for accessibility and utilization of modern interconnecting hardware. Use of troubleshooting procedures and test points can easily identify faulty subassemblies.

6-2. RECOMMENDED SPARE PARTS

Based on reliability and maintainability aspects of design, the following spare parts are recommended for stock at each site for a low quantity of System Noise Monitors:

Item	Description	AILTECH Part Number
	IF Video PC Board	298020-
	Power Supply PC Board	298021-2
	System ENR Gain PC Board	289172-1
	Digital PC Board	298170-1
	Display PC Board	298171-1
S3	Switch, Thumbwheel	299493
F1, 2	Fuse, 1/8 amp (230 VAC connection)	990019-4
	Fuse, 1/4 amp (115 VAC connection)	990019-23
DL2	Lamp, Incandescent	293155

6-3. REPLACEABLE SPARE PARTS

For connector housing service, use Connector Tool supplied by Amp, part number 91084-1.

Main Chassis

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
DL2	Lamp, Incandescent	Data Display	44D57-G0	293155
F1, F2	Fuse, 1/8 amp (230 VAC connection)			990019-4
	Fuse, 1/4 amp (115 VAC connection)			990019-23
FL1	Filter, EMI	Corcom	1EF1	293600
J1	Jack, Panel, Multipin	Cinch	57-40240	294349
J7, J8	Jack, Panel, BNC female		UG-1094A/U	294334
P1	Plug, Cable, Multipin	Cinch	57-30240	294346
P2, P3	Housing, Plug, 10 Pin	Amp	87133-5	299951
P4, P5	Housing, Plug, 20 Pin	Amp	87133-6	299952
P6	Housing, Plug, 10 Pin	Amp	87133-5	299951
P9, P10	Connector, Plug Coaxial Cable	Phelps-Dodge	700156	294392
R4	Resistor, 56.2K, 1%, 1/8 W		RN60C5622F	299709-494
S1	Switch, Paddle, DPDT	C&K Components	7201-J60	294530
S3	Switch, Thumbwheel	Interswitch	IS0905	299493
S8	Switch, Pushbutton	Grayhill	30-3	294519
S11	Switch, Slide, DPDT	Switchcraft	462561FR	294539
	Line Cord, 3 Conductor 6 Ft.	Corcom	80-1245	294948

IF VIDEO PC BOARD (10MHz — 40 MHz) Part Number 298020-1D
(40 MHz — 80 MHz) Part Number 298020-4D

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
C101	Capacitor, 0.01 μF, 50V	TRW	601PE-.01	115285-6
C102	Capacitor, Variable, 15-60 pF	Erie	538-011-F15-60	293747*
C102A	Capacitor, Variable, 1.9-15.7 pF	E. F. Johnson	187-0109-005	293728#
C103	Capacitor, 0.1 μF 50V	TRW	601PE-.1	115285-15
C104 thru C106	Capacitor, 0.001 μF	CRL	DD102	293804
C107	Not Used			
C108 thru C113	Capacitor, 0.001 μF	CRL	DD102	293804
C114, C114A	Capacitor, Variable 15-60 pF	Erie	538011-F15-60	293747
C115, C116	Capacitor, 0.001 μF	CRL	DD102	293804
C117	Capacitor, 470 pF	El Menco	DM15-471J	293840
C118	Capacitor, 0.001 μF	CRL	DD102	293804
C119	Capacitor, 0.01 μF, 50V	TRW	601PE-.01	115285-6
C120	Capacitor, 0.001 μF	CRL	DD102	293804
C121	Capacitor, 470 pF	El Menco	DM15-471J	293840
C122	Capacitor, 0.001 μF	CRL	DD102	293804
C123	Capacitor, 0.01 μF, 50V	TRW	601PE-.01	115285-6
C124, C125	Capacitor, 25 μF, 16V	Sprague	TE1157.1	293883
C126	Capacitor, 0.001 μF	CRL	DD102	293804
C127	Capacitor, 0.1 μF 50V	TRW	601PE-.1	115285-15
C128	Capacitor, 0.001 μF	CRL	DD102	293804
C129, C130	Capacitor, 0.1 μF 50V	TRW	601PE.1	115285-15
C131	Capacitor, 1 μF, 16V	Sprague	TE1148	115307-22
C132	Capacitor, 0.01 μF, 50V	TRW	601PE-.01	115285-6
C133	Capacitor, 0.047 μF	TRW	601PE-.047	115285-14
C134	Capacitor, 1 μF, 16V	Sprague	TE1148	293881
C135	Capacitor, 10 μF, 16V	Sprague	TE1155	115307-16
C136	Capacitor, 2.25 μF	Sprague	CSR13BE225K	293792
C137	Capacitor, 50 μF, 16V	Sprague	TE1160	293884
C138 thru C141	Capacitor, 0.001 μF	CRL	DD102	293804
C142	Not Used			
C143	Capacitor, 10 pF	El Menco	DM5-100J	299241-100
C144	Not Used			
C145	Not Used			
C146	Not Used			

*Used on 298020-1 only
#Used on 298020-4 only

IF VIDEO PC BOARD (continued)

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
C147	Capacitor, 0.1 μF 50V	TRW	601PE-.1	115285-15
C148	Not Used			
C149	Not Used			
C150	Capacitor, 2 μF, 25V	Sprague	TE1201	293885
C151 thru C153	Not Used			
C154	Capacitor, Variable, 15-60 pF	Erie	538-011-F15-60	293747
C158	Capacitor, 0.1 μF, 50V	TRW	601PE-.1	115285-15
CR101	Diode, Semiconductor, Zener		1N936	293241
CR102	Diode, Semiconductor		1N4009	293201
J10	Jack, PC Board, Coaxial, Female	Phelps-Dodge	700214	294396
L101 thru L111	Inductor, 14 μH	Delevan	1840-34	115297-2
L112	Not Used			
L113	Inductor, 0.22 μH	Delevan	1850-04	299237-04#
Q101	Transistor		2N4123	294150
R101	Resistor, 100 Ω, 1/4 W		RC07GF101J	299701-101*
R101A	Resistor, 51 Ω, 1/4 W		RC07GF510J	299701-510#
R102	Resistor, 5.1 K, 1/4 W		RC07GF512J	299701-512
R103	Not Used			
R104	Resistor, Variable, 100 Ω	Bourns	3009P-1-101	299722
R105	Resistor, 10 K, 1/4 W		RC07GF103J	299701-103
R106	Resistor, 510 Ω, 1/4 W		RC07GF511J	299701-511*
R107				
R108, R109	Resistor, 6.2K, 1/4 W		RC07GF622J	299701-622
R110	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R111	Resistor, 1K, 1/4 W		RC07GF102J	299701-102
R112, R113	Resistor, 3.9K, 1/4 W		RC07GF392J	299701-392
R114	Resistor, 10K, 1%, 1/8 W		RN60C1002J	299709-421
R115	Resistor, 100K, 1/4 W		RC07GF104J	299701-104
R116	Resistor, 10K, 1%, 1/8 W		RN60C1002J	299709-421
R117	Resistor, 100K, 1/4 W		RC07GF104J	299701-104
R118 thru R121	Resistor, 1K, 1%, 1/8 W		RN60C1001F	299709-322
R122	Resistor, 7.5K, 1/4 W		RC07GF752J	299701-752

*Used on 298020-1 only
#Used on 298020-4 only

IF VIDEO PC BOARD (continued)

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
R123	Resistor, 1%, 1/8 W	Value Selected At Test	RN60CXXXXF	299709-XXX
R124	Resistor, Variable, 5K	Bourns	3279W-1-502	294091
R125	Resistor, Variable, 20K	Bourns	3279W-1-203	294090
R126	Resistor, 100 Ω, 1%, 1/8 W		RN60C1000F	299709-219
R127	Resistor, 7.50K, 1% 1/8 W		RN60C7501F	299709-409
R128	Resistor, 300 Ω, 1%, 1/8 W		RN60C3000F	299709-667
R129	Resistor, 80.6K, 1%, 1/8 W		RN60C8062F	299709-512
R130	Resistor, 10K, 1%, 1/8 W		RN60C1002J	299709-421
R131	Resistor, 51K, 1/4 W		RC07GF513J	299701-513
R132, R133	Resistor, 100 Ω, 1%, 1/8 W		RN60C1000F	299709-219
R134, R135	Resistor, 20K, 1%, 1/8 W		RN60C2002F	299709-332
R136	Resistor, 1K, 1/4 W		RC07GF102J	299701-102
R137	Resistor, 100K, 1/4 W		RC07GF104J	299701-104
R138	Resistor, 1K, 1/4 W		RC07GF102J	299701-102
R139	Resistor, 1.6K, 1/4 W		RC07GF162J	299701-162
R140	Resistor, Variable, 1K	Bourns	3279W-1-102	299777
R141	Resistor, 1.2K, 1/4 W		RC07GF122J	299701-122
R142	Resistor, 4.3K, 1/4 W		RC07GF432J	299701-432
R143	Resistor, 8.2K, 1/4 W		RC07GF822J	299701-822
R144	Resistor, 4.3K, 1/4 W		RC07GF432J	299701-432
R145	Resistor, 1K, 1/4 W		RC07GF102J	299701-102
R146	Resistor, 820K, 1/4 W		RC07GF824J	299701-824
R147, R148	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R149	Resistor, 200K, 1%, 1/8 W		RN60C2003F	299709-547
R150	Resistor, Variable, 10K	Bourns	3279W-1-103	299778
R151	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R152	Resistor 1M, 1/4 W		RC07GF105J	299701-105
R153	Resistor, 10 Ω, 1/4 W		RC07GF100J	299701-100*
R153A	Resistor, 15 Ω, 1/4 W		RC07GF150J	299701-150#
R154	Resistor, 10 Ω, 1/4 W		RC07GF100J	299701-100*
R154A	Resistor, 15 Ω, 1/4 W		RC07GF150J	299701-150#
R155	Not Used			
R156				
R157	Resistor, Variable, 5K	Bourns	3279W-1-502	294091
R158	Resistor, 2.2K, 1/4 W		RC07GF222J	299701-222
R159	Resistor, 3K, 1/4 W		RC07GF302J	299701-302
R160	Resistor, 1K, 1%, 1/8 W		RN60C1001F	299709-322
R161	Resistor, Variable, 5K	Bourns	3279W-1-502	294091

*Used on 298020-1 only
#Used on 298020-4 only

IF VIDEO PC BOARD (continued)

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
R162, R163	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R164	Resistor, 6.04K, 1%, 1/8 W		RN60C6041F	299709-400
R165	Resistor, 10K, 1%, 1/8 W		RN60C1002J	299709-421
R166	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R167	Resistor, 51K, 1/4 W		RC07GF513J	299701-513
R168	Resistor, 510 Ω, 1/4 W		RC07GF511J	299701-511
R169	Resistor, Variable, 2K	Bourns	3279W-1-202	299779
R170	Resistor, 4.02K, 1%, 1/8 W		RN60C4021F	299709-380
R171	Resistor, 7.5K, 1/4 W		RC07GF752J	299701-752
R172	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R173, R174	Resistor, 82.5K, 1%, 1/8W		RN60C8252F	299709-510
S101, S102	Switch, 14 Pin, DIP	Minelco	SW40-1142	294503
T101	Transformer	Magnetico	12572	298730
T102	Transformer	Magnetico	12419	294809*
T102A	Transformer	Magnetico	12420	294810#
Z101, Z102	Integrated Circuit	Motorola	MC1350P	293395
Z103	Integrated Circuit	Motorola	MC1496L	293498
Z104, Z105	Integrated Circuit	Signetics	UA747CA	293484
Z106	Integrated Circuit	RCA	CD4016AE	293381
Z107	Integrated Circuit	Signetics	UA747CA	293484
Z108	Integrated Circuit	RCA	CD4016AE	293381
Z109	Integrated Circuit	Signetics	UA747CA	293484
Z110	Integrated Circuit	RCA	CD4016AE	293381
Z111	Integrated Circuit	Signetics	UA747CA	293484
Z112	Integrated Circuit	RCA	CD4016AE	293381
Z113	Integrated Circuit	Signetics	UA747CA	293484
Z114	Integrated Circuit	RCA	CD4049AE	293384
Z115, Z116	Integrated Circuit	RCA	CD4000AE	293376
Z117	Integrated Circuit	Signetics	UA747CA	293484

*Used on 298020-1 only
#Used on 298020-4 only

POWER SUPPLY PC BOARD ASSEMBLY
Part Number 298021-2

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
C201	Capacitor, 10 μF, 16V	Sprague	TE1155	115307-16
C202	Capacitor, 1000 μF, 25V	Cornell-Dubilier	BR1000-25	293763
C203	Capacitor, 0.001 μF	Centralab	DD-102	293804
C204	Capacitor, 0.1 μF	Centralab	DDA-104	293820
C205	Capacitor, 10 μF, 16V	Sprague	TE1155	115307-16
C206	Capacitor, 500 μF, 25V	Cornell-Dubilier	BR500-25	293762
C207	Capacitor, 0.1 μF	Centralab	DDA-104	293820
C208	Capacitor, 0.01 μF	Sprague	5HKS-S10	299244
C209	Capacitor, 250 μF, 50V	Cornell-Dubilier	BR250-50	293761
C210	Capacitor, 100 pF	Centralab	DD101	293803
C211	Capacitor, 200 μF, 25V	Cornell-Dubilier	BR2000-25	293764
C212	Capacitor, 10 μF, 16V	Sprague	TE1155	115307-16
CR201 thru CR203	Rectifier, Bridge	General Instrument	W02M	294768
J2, J3	Connector, Post	Amp	86091-2	293079
J4 thru J8	Not Used			
J9	Jack, P.C. Board, Coaxial	Phelps-Dodge	700209	294395
P2, P3	Housing, Plug, 10 Pin	Amp	87133-5	299951
P4 thru P8	Not Used			
P9	Plug, Coaxial	Phelps-Dodge	700156	294392
Q201, Q202	Transistor		2N4123	294150
R201	Resistor, 2 Ω, 1/2 W		RC20GF2R0J	299702-000
R202	Resistor, 1K, 1/4 W		RC07GF102J	299701-102
R203	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
R204	Resistor, 14K, 1%, 1/8 W		RN60C1402F	299709-435
R205	Resistor, Variable, 5K	Weston	502-005-5K	294091
R206, R207	Resistor, 6.81K, 1%, 1/8 W		RN60C6811F	299709-405
R208	Resistor, 16.9K, 1%, 1/8 W		RN60C1692F	299709-443
R209	Resistor, 2 Ω, 1/2 W		RC20GF2R0J	299702-000
R210	Resistor, 15K, 1/4 W		RC07GF153J	299701-153
R211	Resistor, 2K, 1/4 W		RC07GF202J	299701-202
R212	Resistor, 10 Ω, 1/4 W		RC07GF100J	299701-100
R213	Resistor, 5.1K, 1/4 W		RC07GF512J	299701-512
R214	Resistor, 6.81K, 1%, 1/8 W		RN60C6811F	299709-405

POWER SUPPLY PC BOARD ASSEMBLY (continued)

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
R215	Resistor, Variable, 500 Ω	Weston	502-005-500	299780
R216	Resistor, 2.0K, 1%, 1/8 W		RN60C2001F	299709-351
T201	Transformer	Magnetico	50872	294812
Z201	Integrated Circuit	Motorola	MC1469R	293397
Z202	Integrated Circuit	Motorola	MC1463R	293396
Z203	Integrated Circuit	Motorola	MC1723CL	293502
Z204	Integrated Circuit	Fairchild	UGJ7805393	293492

ENR PC BOARD ASSEMBLY
Part Number 298172-1

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
J6	Connector Post	Amp	86091-2	293079
P6	Housing, Plug, 10 Pin	Amp	87133-5	299951
Z501	Integrated Circuit			298259
Z502	Integrated Circuit			298260
	Connector, P.C. Board	Interswitch	CU400354	294301

DIGITAL PC BOARD
Part Number 298170-1

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
C301	Capacitor, 0.01 μF	Kemet	KDP-203YZ-10K	293858
C302	Capacitor, 10 μF, 16V	Sprague	TE1155	115307-16
C303	Capacitor, 0.01 μF	Kemet	KDP-203YZ-10K	293858
C304	Capacitor, 10 μF, 16V	Sprague	TE1155	115307-16
C305	Capacitor, 39 pF	Centralab	DD-390	293811
C306	Capacitor, 0.22 μF	Cornell-Dubilier	MCR/1P22	293863
C307	Capacitor, 1000 pF	Centralab	DD-102	293804
C308	Capacitor, 1000 pF	Corning	TY07-102J	293906
C309	Capacitor, 0.33 μF	Sprague	HY-375	293854
C310	Capacitor, 0.02 μF	Centralab	DD-203	293809
CR301	Diode, Semiconductor, Zener, 4.7V		1N750A	293234
CR302	Diode, Semiconductor, Zener, 6.0V		1N706A	293230
R301	Resistor, Variable, 500Ω	Bourns	3279W-1-501	294091-2
R302	Resistor, 5.11K, 1%, 1/8 W		RN60C5111F	299709-393
R303	Resistor, 1.24K, 1%, 1/8 W		RN60C1241F	299709-331
R304	Resistor, 10K, 1%, 1/8 W		RN60C1002F	299709-421
R305	Not Used			
R306	Resistor, 24.3K, 1%, 1/8 W		RN60C2432F	299709-458
R307	Resistor, 806 Ω, 1%, 1/8 W		RN60C8060F	299709-312
R308	Resistor, 51.1K, 1%, 1/8 W		RN60C5112F	299709-490
R309	Resistor, 2.21K, 1%, 1/8 W		RN60C2211F	299709-355
R310	Resistor, 113K, 1%, 1/8 W		RN60C1133F	299709-523
R311, R312	Resistor, 243K, 1%, 1/8 W		RN60C2433F	299709-555
R313	Resistor, Variable, 500Ω	Bourns	3279W-1-501	294091-2
R314	Resistor, 2.74K, 1%, 1/8 W		RN60C2741F	299709-364
R315	Resistor, 750Ω, 1/4 W		RC07GF751J	299701-751
R316	Resistor, 220K, 1/4 W		RC07GF224J	299701-224
R317	Resistor, 113K, 1%, 1/8 W		RN60C1133F	299709-523
R318	Resistor, 12K, 1/4 W		RC07GF123J	299701-123
R319	Resistor, 5.1K, 1/4 W		RC07GF512J	299701-512
R320	Resistor, Variable, 500Ω		3279W-1-501	294091-2
R321	Resistor, 562Ω, 1%, 1/8 W		RN60C5620F	299709-296
R322	Resistor, 1.5K, 1/4 W		RC07GF152J	299701-152
R323, R324	Resistor, 200Ω, 1/4 W		RC07GF201J	299701-201
R325	Resistor, 390Ω, 1/4 W		RC07GF391J	299701-391
R326	Resistor, 4.3K, 1/4 W		RC07GF432J	299701-432
R327	Resistor, Variable, 1K	Bourns	3279W-1-102	299777
R328	Resistor, 4.02K, 1%, 1/8 W		RN60C4021F	299709-380
R329	Resistor, Variable, 500Ω	Bourns	3279W-1-501	294091-2

DIGITAL PC BOARD (continued)

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
R330	Resistor, 1.2K, 1/4 W		RC07GF122J	299701-122
R331 thru R338	Resistor, 5.1K, 1/4 W		RC07GF512J	299701-512
R339	Resistor, 100K, 1/4 W		RC07GF104J	299701-104
R340	Resistor, 5.1K, 1/4 W		RC07GF512J	299701-512
R341 thru R346	Resistor, 10K, 1/4 W		RC07GF103J	299701-103
Z301 thru Z303	Integrated Circuit	Texas Instruments	SN72741N	293463
Z304	Integrated Circuit	Texas Instruments	SN72710N	293462
Z305	Integrated Circuit	Intersil	IH5012C-PE	293387
Z306, Z307	Integrated Circuit	Intersil	IH5014C-PD	293388
Z308	Integrated Circuit	Texas Instruments	SN74L74N	293430
Z309	Integrated Circuit	Texas Instruments	SN74L00N	293421
Z310, Z311	Integrated Circuit	Texas Instruments	SN74L93N	293434
Z312	Integrated Circuit	Texas Instruments	SN74L00N	293421
Z313, Z314	Integrated Circuit	Texas Instruments	SN74L93N	293434
Z315	Integrated Circuit	Texas Instruments	SN74L04N	293424
Z316	Integrated Circuit	Texas Instruments	SN74L20N	293426
Z317	Integrated Circuit	Texas Instruments	SN74L30N	293427
Z318	Integrated Circuit	Texas Instruments	SN74L04N	293424
Z319	Integrated Circuit	Texas Instruments	SN7400N	293366
Z320 thru Z322	Integrated Circuit	Texas Instruments	SN74L10N	293424
Z323	ROM	National Semiconductor	MM5232BCH	293406
Z324	Not Used			
Z325 thru Z327	Integrated Circuit	Texas Instruments	SN74L75N	293431
Z328	Integrated Circuit	Texas Instruments	SN74L00N	293366
Z329, Z330	Integrated Circuit	Texas Instruments	SN74L03N	293423
Z331	Integrated Circuit	Texas Instruments	SN74L02N	293362
Z332	Integrated Circuit	Texas Instruments	SN74L20N	293426
Z333	Integrated Circuit		SN74L30N	293427

DISPLAY BOARD ASSEMBLY
Part Number 298171-1

Item	Description	Manufacturer	Manufacturer Part Number	AILTECH Part Number
D401, D402, D403	Display, LED	Opcoa	SLA-1	293217
I401	Not Used			
I402	Lamp	Lamps, Inc.	455	293161
J16	Post	Amp	86091-4	293079
J17	Post	Amp	86091-4	293079
R401 thru R424	Resistor, 300Ω, 1/4 W		RC07GF301J	299701-301
Z401, Z402, Z403	Integrated Circuit		SN74L47	293429

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